YUZHE MA

Assistant Professor ◇ Microelectronics Thrust
The Hong Kong University of Science and Technology (Guangzhou)
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RESEARCH INTERESTS

- Electronic design automation
- Machine learning-aided VLSI design
- Domain-specific architecture design
- Hardware-friendly learning algorithms

EDUCATION

The Chinese University of Hong Kong Aug. 2016 – Jul. 2020
Ph.D. Computer Science & Engineering

Sun Yat-Sen University Sep. 2011 – Jul. 2016
B.Eng. Microelectronics

EXPERIENCE

Assistant Professor Dec. 2021 – Present
The Hong Kong University of Science and Technology (Guangzhou)
Guangzhou, China

Senior Research Scientist Sep. 2020 – Nov. 2021
Huawei Hong Kong Research Center
Hong Kong SAR, China

Research Intern June 2019 – Feb. 2020
YouTu Lab, Tencent
Shenzhen, China

Research Intern Jul. 2018 – Nov. 2018
ASIC and VLSI Research Group, NVIDIA Research
Austin, TX, USA

Research Intern May 2017 – Sep. 2017
Innovus Team, Cadence Design Systems Inc.
San Jose, CA, USA

SELECTED AWARDS AND HONORS

Best Paper Award	ICCAD	2021
Best Paper Award	ASPDAC	2021
Best Poster (Research) Award	ASPDAC SRF, ACM SIGDA	2020
Third Place Award	ISPD Contest	2020
Best Student Paper Award	ICTAI	2019
Best Paper Award Nomination	ASPDAC	2019

PUBLICATIONS

Journal Papers

[J21] Ziyang Yu, Peiyu Liao, **Yuzhe Ma**, Bei Yu, Martin D.F. Wong, "CTM-SRAF: Continuous Transmission Mask-based Constraint-aware Sub Resolution Assist Feature Generation", accepted by IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**).

[J20] **Yuzhe Ma**, Xufeng Yao, Ran Chen, Ruiyu Li, Xiaoyong Shen, Bei Yu, "Small is Beautiful: Compressing Deep Neural Networks for Partial Domain Adaptation", accepted by IEEE Transactions on Neural Networks and Learning Systems (**TNNLS**).

[J19] Ziyang Yu, Guojin Chen, **Yuzhe Ma**, Bei Yu, "A GPU-enabled Level Set Method for Mask Optimization", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**), vol. 42, no. 02, pp. 594–605, 2023

[J18] Hao Geng, Tinghuan Chen, **Yuzhe Ma**, Binwu Zhu, Bei Yu, "PTPT: Physical Design Tool Parameter Tuning via Multi-Objective Bayesian Optimization", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**), vol. 42, no. 01, pp. 178-–189, 2023.

[J17] Xiaodong Wang, Changhao Yan, **Yuzhe Ma**, Bei Yu, Fan Yang, Dian Zhou, Xuan Zeng, "Analog Circuit Yield Optimization via Freeze-Thaw Bayesian Optimization Technique", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**), vol. 41, no. 11, pp. 4887–4900, 2022.

[J16] Wei Li, **Yuzhe Ma**, Yibo Lin, Bei Yu, "Adaptive Layout Decomposition with Graph Embedding Neural Networks", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**), vol. 41, no. 11, pp. 5030–5042, 2022.

[J15] Guojin Chen, Wanli Chen, Qi Sun, **Yuzhe Ma**, Haoyu Yang, Bei Yu, "DAMO: Deep Agile Mask Optimization for Full Chip Scale", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**), vol. 41, no. 9, pp. 3118–3131, 2022.

[J14] Hao Geng, **Yuzhe Ma**, Qi Xu, Jin Miao, Subhendu Roy, Bei Yu, "High-Speed Adder Design Space Exploration via Graph Neural Processes", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**), vol. 41, no. 8, pp. 2657–2670, 2022.

[J13] Bentian Jiang, Lixin Liu, **Yuzhe Ma**, Bei Yu, Evangeline F.Y. Young, "Neural-ILT 2.0: Migrating ILT to Domain-specific and Multi-task-enabled Neural Network", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**), vol. 41, no. 8, pp. 2671–2684, 2022.

[J12] Wei Zhong, Shuxiang Hu, **Yuzhe Ma**, Haoyu Yang, Xiuyuan Ma, Bei Yu, "Deep Learning-Driven Simultaneous Layout Decomposition and Mask Optimization", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**), vol. 41, no. 3, pp. 709—722, 2022.

[J11] Wei Li, **Yuzhe Ma**, Qi Sun, Lu Zhang, Yibo Lin, Iris Hui-Ru Jiang, Bei Yu, David Z. Pan, "OpenMPL: An Open Source Layout Decomposer", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**), vol. 40, no. 11, pp. 2331—2344, 2021.

[J10] Guyue Huang, Jingbo Hu, Yifan He, Jialong Liu, Mingyuan Ma, Zhaoyang Shen, Juejian Wu, Yuanfan Xu, Hengrui Zhang, Kai Zhong, Xuefei Ning, **Yuzhe Ma**, Haoyu Yang, Bei Yu, Huazhong Yang, Yu Wang, "Machine Learning for Electronic Design Automation: A Survey", ACM Transactions on Design Automation of Electronic Systems (**TODAES**), vol. 25, no. 5, 2021.

[J9] Haoyu Yang, Wei Zhong, **Yuzhe Ma**, Hao Geng, Ran Chen, Wanli Chen, Bei Yu, "VLSI Mask Optimization: From Shallow To Deep Learning", Integration, the VLSI Journal, vol. 77, Mar., pp. 96–103, 2021.

[J8] Kang Liu, Haoyu Yang, **Yuzhe Ma**, Benjamin Tan, Bei Yu, Evangeline F. Y. Young, Ramesh Karri, Siddharth Garg, "Are Adversarial Perturbations a Showstopper for ML-Based CAD? A Case Study on CNN-Based Lithographic Hotspot Detection", ACM Transactions on Design Automation of Electronic Systems (**TODAES**), vol. 25, no. 5, 2020.

[J7] **Yuzhe Ma**, Wei Zhong, Shuxiang Hu, Jhih-Rong Gao, Jian Kuang, Jin Miao, Bei Yu, "A Unified Framework for Simultaneous Layout Decomposition and Mask Optimization", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**), vol. 39, no. 12, pp. 5069–5082, 2020.

[J6] Hao Geng, Wei Zhong, Haoyu Yang, **Yuzhe Ma**, Joydeep Mitra, Bei Yu, "SRAF Insertion via Supervised Dictionary Learning", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**), vol. 39, no. 10, pp. 2849–2859, 2020.

[J5] Haoyu Yang, Shuhe Li, Zihao Deng, **Yuzhe Ma**, Bei Yu, and Evangeline F. Y. Young, "GAN-OPC: Mask Optimization with Lithography-guided Generative Adversarial Nets", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**), vol. 39, no. 10, pp. 2822–2834, 2020.

[J4] **Yuzhe Ma**, Subhendu Roy, Jin Miao, Jiamin Chen, and Bei Yu, "Cross-layer Optimization for High Speed Adders: A Pareto Driven Machine Learning Approach", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**), vol. 38, no. 12, pp. 2298–2311, 2019

[J3] Qianru Zhang, Meng Zhang, Tinghuan Chen, Zhifei Sun, **Yuzhe Ma**, and Bei Yu, "Recent Advances in Convolutional Neural Network Acceleration", Neurocomputing, vol. 323, pp. 37-51, Jan., 2019.

[J2] Haoyu Yang, Jing Su, Yi Zou, **Yuzhe Ma**, Bei Yu, and Evangeline F. Y. Young, "Layout Hotspot Detection with Feature Tensor Generation and Deep Biased Learning", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**), vol. 38, no. 6, pp. 1175–1187, 2019.

[J1] Jin Miao, Meng Li, Subhendu Roy, **Yuzhe Ma**, and Bei Yu, "SD-PUF: Spliced Digital Physical Unclonable Function", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**), vol. 37, no. 5, pp. 927–940, 2018.

Conference Papers

[C30] Dongsheng Zuo, Yikang Ouyang, **Yuzhe Ma**, "RL-MUL: Multiplier Design Optimization with Deep Reinforcement Learning", ACM/IEEE Design Automation Conference (**DAC**), San Francisco, Jul. 09-13, 2023.

[C29] Zhuolun He, Yihang Zuo, Jiaxi Jiang, Haisheng Zheng, **Yuzhe Ma**, Bei Yu, "OpenDRC: An Efficient Open-Source Design Rule Checking Engine with Hierarchical GPU Acceleration", ACM/IEEE Design Automation Conference (**DAC**), San Francisco, Jul. 09-13, 2023.

[C28] Guojin Chen, Zehua Pei, Haoyu Yang, **Yuzhe Ma**, Bei Yu, Martin Wong, "Physics-Informed Optical Kernel Regression Using Complex-valued Neural Fields", ACM/IEEE Design Automation Conference (**DAC**), San Francisco, Jul. 09-13, 2023.

[C27] Zhuolun He, **Yuzhe Ma**, Bei Yu, "X-Check: GPU-Accelerated Design Rule Checking via Parallel Sweepline Algorithms", IEEE/ACM International Conference on Computer-Aided Design (**ICCAD**), San Diego, Oct. 30-Nov. 3, 2022.

[C26] Wenqian Zhao, Xufeng Yao, Ziyang Yu, Guojin Chen, **Yuzhe Ma**, Bei Yu, Martin Wong, "AdaOPC: A Self-Adaptive Mask Optimization Framework For Real Design Patterns", IEEE/ACM International Conference on Computer-Aided Design (**ICCAD**), San Diego, Oct. 30-Nov. 3, 2022.

[C25] Chen Bai, Qi Sun, Jianwang Zhai, **Yuzhe Ma**, Bei Yu, Martin D.F. Wong, "BOOM-Explorer: RISC-V BOOM Microarchitecture Design Space Exploration Framework", IEEE/ACM International Conference on Computer-Aided Design (**ICCAD**), Nov. 01-04, 2021. **(William J. McCalla Best Paper Award)**

[C24] Guojin Chen, Ziyang Yu, Hongduo Liu, **Yuzhe Ma**, Bei Yu, "DevelSet: Deep Neural Level Set for Instant Mask optimization", IEEE/ACM International Conference on Computer-Aided Design (**ICCAD**), Nov. 01-04, 2021.

[C23] Junzhe Cai, Changhao Yan, **Yuzhe Ma**, Bei Yu, Dian Zhou, Xuan Zeng "DevelSet: Deep Neural Level Set for Instant Mask optimization", ACM/IEEE Design Automation Conference (**DAC**), San Francisco, Dec. 5-9, 2021.

[C22] Ziyang Yu, Guojin Chen, **Yuzhe Ma**, Bei Yu, "A GPU-enabled Level-Set Method for Mask Optimization", IEEE/ACM Proceedings Design, Automation and Test in Europe (**DATE**), Feb. 01-05, 2021.

[C21] Zhuolun He, Peiyu Liao, Siting Liu, **Yuzhe Ma**, Bei Yu, "Physical Synthesis for Advanced Neural Network Processors", IEEE/ACM Asian and South Pacific Design Automation Conference (**ASPDAC**), Jan. 18-21, 2021. (Invited Paper)

[C20] Wei Li, Yuxiao Qu, Gengjie Chen, **Yuzhe Ma**, Bei Yu, "TreeNet: Deep Point Cloud Embedding for Routing Tree Construction", IEEE/ACM Asian and South Pacific Design Automation Conference (**ASPDAC**), Jan. 18-21, 2021. **(Best Paper Award)**

[C19] Zhuolun He, Lu Zhang, Peiyu Liao, **Yuzhe Ma**, Bei Yu, "Reinforcement Learning Driven Physical Synthesis", IEEE International Conference on Solid -State and Integrated Circuit Technology (**ICSICT**), Nov. 3-6, 2020. (Invited Paper)

[C18] Guojin Chen, Wanli Chen, **Yuzhe Ma**, Haoyu Yang, Bei Yu, "DAMO: Deep Agile Mask Optimization for Full Chip Scale", IEEE/ACM International Conference on Computer-Aided Design (**ICCAD**), Nov. 2-5, 2020.

[C17] Bentian Jiang, Lixin Liu, **Yuzhe Ma**, Hang Zhang, Evangeline F. Y. Young, Bei Yu, "Neural-ILT: Migrating ILT to Nerual Networks for Mask Printability and Complexity Co-optimizaton", IEEE/ACM International Conference on Computer-Aided Design (**ICCAD**), Nov. 2-5, 2020.

[C16] Zhuolun He, **Yuzhe Ma**, Lu Zhang, Peiyu Liao, Ngai Wong, Bei Yu, Martin D. F. Wong, "Learn to Floorplan through Acquisition of Effective Local Search Heuristics", IEEE International Conference on Computer Design (**ICCD**), Oct. 18–21, 2020.

[C15] Wei Li, Jialu Xia, **Yuzhe Ma**, Jialu Li, Yibo Lin, Bei Yu, "Adaptive Layout Decomposition with Graph Embedding Neural Networks", ACM/IEEE Design Automation Conference (**DAC**), San Francisco, CA, July 19–23, 2020.

[C14] Wei Zhong, Shuxiang Hu, **Yuzhe Ma**, Haoyu Yang, Xiuyuan Ma, Bei Yu, "Deep Learning-Driven Simultaneous Layout Decomposition and Mask Optimization", ACM/IEEE Design Automation Conference (**DAC**), San Francisco, CA, July 19–23, 2020.

[C13] **Yuzhe Ma**, Zhuolun He, Wei Li, Tinghuan Chen, Lu Zhang, Bei Yu, "Understanding Graphs in EDA: From Shallow to Deep Learning", ACM International Symposium on Physical Design (**ISPD**), Taipei, Mar. 25–Apr. 01, 2020. (Invited Paper)

[C12] Haoyu Yang, Wei Zhong, **Yuzhe Ma**, Hao Geng, Ran Chen, Wanli Chen, Bei Yu, "VLSI Mask Optimization: From Shallow To Deep Learning", IEEE/ACM Asian and South Pacific Design Automation Conference (**ASPDAC**), Beijing, Jan. 13–16, 2020. (Invited Paper)

[C11] Zhonghua Zhou, Ziran Zhu, Jianli Chen, **Yuzhe Ma**, Bei Yu, Tsung-Yi Ho, Guy Lemieux, Andre Ivano, "Congestion-aware Global Routing using Deep Convolutional Generative Adversarial Networks", ACM/IEEE Workshop on Machine Learning for CAD (**MLCAD**), Alberta, Canada, Sep. 3–4, 2019.

[C10] **Yuzhe Ma**, Ziyang Yu, Bei Yu, "CAD Tool Design Space Exploration via Bayesian Optimization", ACM/IEEE Workshop on Machine Learning for CAD (**MLCAD**), Alberta, Canada, Sep. 3–4, 2019.

[C9] **Yuzhe Ma**, Ran Chen, Wei Li, Fanhua Shang, Wenjian Yu, Minsik Cho, Bei Yu, "A Unified Approximation Framework for Compressing and Accelerating Deep Neural Networks", IEEE International Conference on Tools with Artificial Intelligence (**ICTAI**), Portland, OR, Nov. 4–6, 2019. **(Best Student Paper Award)**

[C8] Wei Li, **Yuzhe Ma**, Qi Sun, Yibo Lin, Iris Hui-Ru Jiang, Bei Yu, David Z. Pan, "OpenMPL: An Open Source Layout Decomposer", IEEE International Conference on ASIC (**ASICON**), Chongqing, China, Oct. 29–Nov. 1, 2019.

[C7] **Yuzhe Ma**, Haoxing Ren, Brucek Khailany, Harbinder Sikka, Karthikeyan Natarajan, and Bei Yu, "High Performance Graph Convolutional Networks with Applications in Testability Analysis", ACM/IEEE Design Automation Conference (**DAC**), Las Vegas, NV, June 2–6, 2019.

[C6] Hao Geng, Haoyu Yang, **Yuzhe Ma**, Joydeep Mitra, and Bei Yu, "SRAF Insertion via Supervised Dictionary Learning", IEEE/ACM Asian and South Pacific Design Automation Conference (**ASPDAC**), Tokyo, Jan. 21–24, 2019. **(Best Paper Award Nomination)**

[C5] Haoyu Yang, Shuhe Li, **Yuzhe Ma**, Bei Yu, and Evangeline F. Y. Young, "GAN-OPC: Mask Optimization with Lithography-guided Generative Adversarial Nets", ACM/IEEE Design Automation Conference (**DAC**), San Francisco, CA, June 24–28, 2018.

[C4] **Yuzhe Ma**, Jhih-Rong Gao, Jian Kuang, Jin Miao, and Bei Yu, "A Unified Framework for Simultaneous Layout Decomposition and Mask Optimization", IEEE/ACM International Conference on Computer-Aided Design (**ICCAD**), Irvine, CA, Nov. 13–16, 2017.

[C3] Chak-Wa Pui, Gengjie Chen, **Yuzhe Ma**, Evangeline F. Y. Young, and Bei Yu, "Clock-Aware UltraScale FPGA Placement with Machine Learning Routability Prediction", IEEE/ACM International Conference on Computer-Aided Design (**ICCAD**), Irvine, CA, Nov. 13–16, 2017.

[C2] **Yuzhe Ma**, Xuan Zeng, and Bei Yu, "Methodologies for Layout Decomposition and Mask Optimization: A Systematic Review", IFIP/IEEE International Conference on Very Large Scale Integration (**VLSI-SoC**), Abu Dhabi, UAE, Oct. 23–25, 2017.

[C1] Subhendu Roy, **Yuzhe Ma**, Jin Miao, and Bei Yu, "A Learning Bridge from Architectural Synthesis to Physical Design for Exploring Power Efficient High-Performance Adders", IEEE/ACM International Symposium on Low Power Electronics and Design (**ISLPED**), Taipei, Taiwan, July 24–26, 2017.

Patents

[P1] **Yuzhe Ma**, Haoxing Ren, Brucek Khailany, Harbinder Sikka, Lijuan Luo, Karthikeyan Natarajan, "Deep Learning Testability Analysis with Graph Convolutional Networks", US Patent 10657306, May, 2020.

TEACHING/TEACHING ASSISTANT

Spring 2019	Energy Efficient Computing
Spring 2018	Practical Computational Geometry Algorithms
Spring 2017	Approximation Algorithms
Fall 2016, 2017	Embedded System Development and Applications

PROFESSIONAL SERVICE

Selected TPC Member

- ACM/IEEE Design Automation Conference (DAC), 2022, 2023
- IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2022
- IEEE Asia Pacific Conference on Circuits and Systems (APCCAS), 2022
- IEEE International Conference on Artificial Intelligence Circuits and Systems (AICAS), 2022
- Workshop on Synthesis And System Integration of Mixed Information Technologies (SASIMI), 2021, 2022

Journal Reviewer

- IEEE Transaction on Computer-Aided Design of Integrated Circuits and Systems (TCAD)
- ACM Transaction on Design Automation of Electronic Systems (TODAES)
- ACM Transaction on Cyber-Physical Systems (TCPS)
- IEEE Transactions on Very Large Scale Integration (VLSI) Systems
- VLSI Design
- IET Cyber-Physical Systems: Theory & Applications

Invited/External Conference Reviewer

- IEEE Conference on Computer Vision and Pattern Recognition (CVPR), 2020, 2021
- ACM/IEEE Design Automation Conference (DAC), 2018, 2019, 2020
- AAAI Conference on Artificial Intellignece (AAAI), 2021, 2022
- ACM International Symposium on Physical Design (ISPD), 2018, 2019
- IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC), 2018