PowerSoC User Manual

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Due to the power dissipation limitation of transistors, many-core processor system becomes promising to improve system performance and power efficiency instead of feature size scaling alone. Power delivery system is a key subsystem within it, which has important influence towards its performance and power consumption. Conventional voltage regulators are contained in board-level modules with large inductors or capacitors, which slow down the responding time of their feedback control. The costs and sizes of the capacitors and inductors also severely limit their usage for fine-grained power domain regulation [1]. Hence, there has been a surge of interest to implement on-chip voltage regulators, especially the on-chip buck converters [2] [3] [4]. However, the on-chip voltage regulators doesn't come for free. If the voltage regulator is integrated on-chip, the output voltage drops much more in response to the load current step than its off-chip counterpart [1]. Because this on-chip capacitor is much smaller, large load current steps can rapidly drain out the limited charge stored on the capacitor before the converter loop can respond. The on-chip voltage regulators also introduce the power loss and area overhead. Hence, there is a need of a design optimization and analysis platform to systematically evaluate these pros and cons and conduct the design of the next-generation power delivery system involving both on/off-chip voltage regulators. In this project, we will introduce the PowerSoC, which is short for Power Supply On-Chip. It is a design optimization and analysis platform of power supply targeted to fast and accurately evaluate the important characteristics of the complex power delivery system including both on/off-chip voltage regulators and power delivery network for multi-core processors. PowerSoC is based on the analytical study of the power delivery system using on/off-chip voltage regulators presented in our previous work. PowerSoC is a $C++$ based program to analyze the important characteristics of power delivery system, e.g. power efficiency, area and transient response, and optimize the complex power delivery system design to tradeoff among those important characteristics. The overview of PowerSoC is illustrated in Fig. 1. The inputs to the platform include the device parameters of the on/off-chip voltage regulators including the transistors, capacitors and inductors, the parameters of the power delivery network, and the configuration, temperature distribution and design constraints of power supply system. The voltage regulator library includes several typical designs of different kinds of voltage regulators. Based on the detailed models of the voltage regulators and power delivery network, a geometric programming based optimization strategy will be used to efficient explore the design space and guide the power supply system design. PowerSoC models the steady state and transient response of different components of the power supply system.

I. Model of power delivery system

The multi-stage power delivery system using both off-chip and on-chip voltage regulators becomes promising. A two-stage power delivery system is illustrated in Figure 2. Given an inherent degradation in power efficiency for large conversion ratios, the first stage of off-chip voltage regulators performs the initial step-down to an intermediate voltage. The intermediate power supply then drives the second stage, on-chip voltage regulators, down to the core voltage. The number of the voltage regulators varies with different granularity to provide at most one power domain per core.

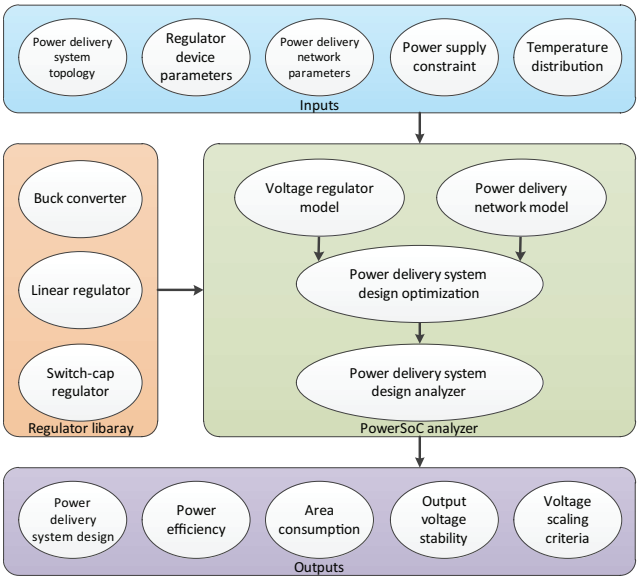

Fig. 1: The overview of PowerSoC

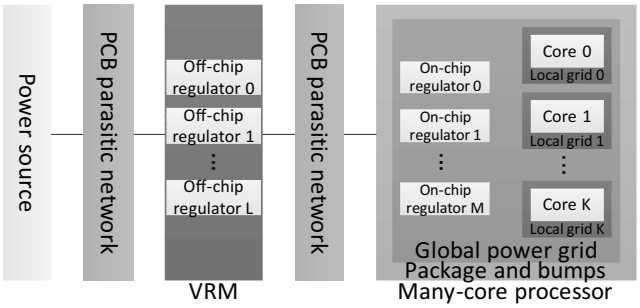

Fig. 2: Overview of a two-stage power delivery system

A. Model of Switching Mode Voltage Regulators

The characteristics of the voltage regulators have significant influence towards the entire power delivery system, e.g. power efficiency, transient response. Interleaved multi-phase buck converter becomes popular to supply high-current processors because of the lower input and output current ripple and fast transient response. The primary building blocks of a multi-phase buck converter is shown in Fig. 3. Similar phases of the buck converters will be operated in parallel with a common output capacitor. By applying a $360°/N$ phase difference between sawtooth waves of the adjacent phases, the output current ripple can be canceled out while maintaining the fast transient response. N is the number of the parallel phases. Because we focus on high performance many-core processors, continuous mode operation of converters is assumed when analyzing the characteristics.

Power efficiency is one of the important features of voltage regulators, which directly influences the power efficiency of the power delivery system. There are some important power losses which are usually considered in the literatures about the buck converter modeling, e.g. the switching loss of the power bridge and corresponding driver circuits, resistive loss of the power bridge, resistive loss of the inductor and the power of the control circuits [4] [5]. The estimation of those power losses of one phase is presented as follows:

$$P_{driver} = C_{driver} V_{driver}^2 f_{sw} \tag{1}$$

$$P_{R_{ds}} = R_{ds}(I_{ind}^2 + \frac{\Delta I_{ind}^2}{12}) \tag{2}$$

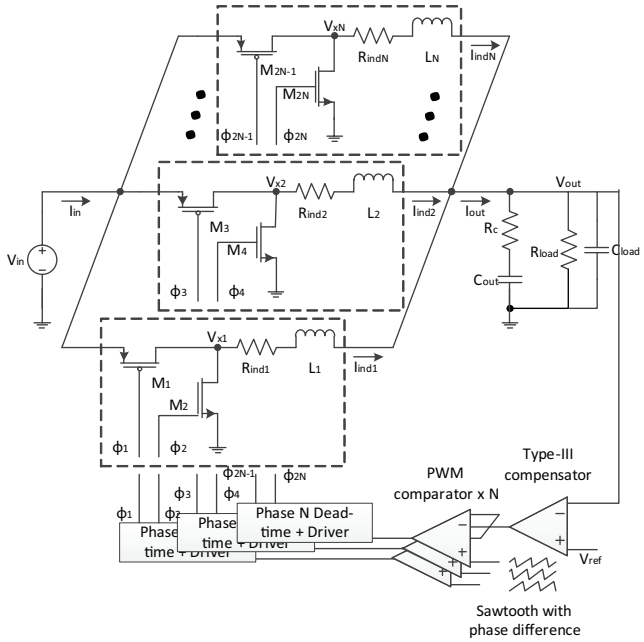

Fig. 3: Simplified block diagram of multi-phase interleaved buck converters

$$P_{R_{ind}} = R_{ind}(I_{ind}^2 + \frac{\Delta I_{ind}^2}{12}) \tag{3}$$

$$P_{control} = I_{control} V_{driver} \tag{4}$$

where C_{driver} is the effective switched capacitance of the drivers and power bridge, and f_{sw} is the switching frequency. The switching capacitance is estimated by including the gate and diffusion capacitance of the transistors, and C_{driver} is derived by summarizing the switched capacitance of all the stages in the entire buffer chain of driver circuit and power bridge. The size of the drivers is designed to be fan-out of 4. V_{driver} is the supply voltage of the drivers and control logic. It may be different from the input voltage V_{in} for off-chip converters and on-chip converters with high input voltage to reduce the power loss of the driver circuit. Those buck converters use two n-channel MOSFETs as the power bridge, and additional circuits, e.g. level shift and bootstrap circuit, are implemented in the driver circuit [6]. R_{ds} are the on-resistance of the high-side and low-side transistors of the bridge, which are assumed to be equal by adjusting their channel widths. R_{ind} is the equivalent series resistance of the inductor. D is the duty ratio of the gate signal. I_{ind} and ΔI_{ind} are the average value and the peak-to-peak value of the inductor current. $I_{control}$ stands for the supply current of the control circuit of each phase. The other variables can be derived based on principles of buck converters in Eq. 5 and 6.

$$D = \frac{V_{out}}{V_{in}} \frac{R_{ind} + DR_{ds,h} + (1-D)R_{ds,l} + R_{load}}{R_{load}} \tag{5}$$

$$\Delta I_{ind} = \frac{(V_{in} - V_{out})D}{f_{sw} L_{ind}} \tag{6}$$

Besides the power losses above, there are some other power losses that are usually neglected, e.g. static power loss and switching power loss. However, it is observed that some of them may be significant during the design space exploration. Hence, they are considered in our analytical model to improve the accuracy. Static power loss is induced by leakage current of the transistors. The static power loss is included in our model, and the leakage current of the transistors per unit width is estimated by numerical fitting from SPICE simulations as a function of supply voltages. Simple circuits, e.g. the inverters with different

transistor channel widths and supply voltages, are used to estimate the relationship between the leakage current and supply voltage based on the SPICE simulations.

Switching power loss is induced by the current flowing through the transistors of the power bridge during its transition [7]. It mainly consists of the direct path loss and the ringing loss. If both high-side and low-side transistors of the power bridge have a common gate signal, then the power supply terminals will be shorted through the transistors for a short duration. It is called the direct path loss. Most switching schemes incorporate dead-time control to ensure both transistors are not conducting for any period of time, and make direct path loss negligible. The dead-time control scheme is considered to improve the power efficiency [8]. However, the ringing loss may be significant for the conventional synchronous buck converter designs [7]. This happens at the instant the power bridge transistors is switching, because the load current and drain-source voltage of the transistor may not go to zero at the same time. The current spike through the power bridge transistors will fluctuate until the ringing is completely damped. It will induce additional power loss due to the ringing current spike. Small testing circuits are built, and the ringing loss is estimated based on SPICE simulations. It is calculated by integrating the energy pumped from the input source until the current oscillation is completed damped with the deduction of the load power during this transition period. Hence, we are able to develop an analytical model to characterize the power consumption of the converters in Eq. 7.

$$V_{in}I_{in} = V_{out}NI_{ind} + N(P_{driver} + P_{R_{ds}} + P_{R_{ind}} + P_{stat} + P_{sw} + P_{control}) \tag{7}$$

Besides the power efficiency of the converters, there are other important characteristics which affect the cost and the reliability, e.g. the area and output voltage stability. Output ripple is one criterion of the output voltage stability. In order to calculate the influence of the output capacitor and the number of working phases, some concepts concerning the multiple interleaving should be considered. The output current ripple cancelation due to interleaving technique depends on the number of phases N, and improves with more phases in parallel. Assuming that all of the ripple components of the output current flows through the filter capacitor C_{out}, the worst case peak-to-peak output voltage ripple with multiple phases is derived [9]. C_{load} is the parasitic capacitance contributed by the load circuit of the supported power domain, e.g. the processor cores [10]. The second term represents the ripple current cancelation effect of the interleaving technique.

$$\Delta V_{out,ripple} = \frac{\Delta I_{ind}}{8f_{sw}(C_{out} + C_{load})} \frac{0.25}{D(1-D)} \frac{1}{N^2} \tag{8}$$

Load transient response is another important criterion to maintain the stability of supply voltage, which determines how much the voltage fluctuates in response to a current change. If the converters is integrated on-chip, the output voltage of the on-chip converter drops much more in response to the load current step than its off-chip counterpart. Because the output capacitor of on-chip voltage regulator is much smaller than the total decoupling and filter capacitance used for off-chip converters, large load current steps can rapidly drain out the limited charge stored on the capacitor before the converter loop can respond, resulting in a large voltage drop. Hence, there is a need to evaluate the transient voltage drop for the stability of output voltages. The maximum voltage drop is derived in Eq. 9 [11]. The worst case transient voltage drop tends to approach the open-loop value, when the feedback loop response of the control logic is sluggish. α is an user-specified empirical factor to bring the open-loop estimation into agreement with the actual voltage drop. It changes with the response time of the control strategy of converters.

$$\Delta V_{out,tr} = \alpha \cdot \Delta I_{out,tr} \cdot \sqrt{\frac{L_{ind}}{C_{out} + C_{load}}} \tag{9}$$

Voltage scaling performance is another important characteristic of converters, which influence the effectiveness of dynamic voltage scaling based power management. When the output voltage scales to a

new voltage level, it scales gradually. To ensure sufficient timing margins for the processor, the upscaling first attempts voltage scaling and waits until the voltage is stabilized. Once the voltage is stabilized, the processor changes the clock frequency. Downsacling is the opposite. The clock frequency is changed first, and the voltage is scaled latter. This sequence is commonly used in the modern processor with the power management of dynamic voltage scaling. At system level, there are two important features about the dynamic voltage scaling. One is the settling time of voltage scaling, which affects the granularity of the timescales of dynamic voltage scaling. The other is the energy loss, including the converter induced energy overhead and the underclocking related loss. The optimum settling time is derived according to the minimum time control law [12]. D_{min} is the average of the duty cycles of the initial and final state of the voltage scaling, and ΔD is the difference between these duty cycles. The voltage mode feedback control can not achieve the optimum settling time. β is used as an user-specified empirical factor to fit the practical settling time of the converters. The settling time is proportional to the product of L_{ind} and C_{out} of the output filter, while the output ripple decreases with larger inductance and capacitance. The tradeoff between these two features is achieved using the optimization strategy.

$$T_{scale} = \beta\sqrt{\frac{2L_{ind}(C_{out}+C_{load})\Delta D}{D_{min}(1-D_{min})(1+0.5\Delta D)}} \tag{10}$$

Voltage scaling will also induce energy overhead, which is divided into two parts [10]. One is the converter induced energy overhead, when a large surge current flows into and out of C_{out} via the inductor and transistors of power bridge. If the output voltage of the final state, $V_{out,fin}$, is higher than the initial one, $V_{out,int}$, the stored energy on the capacitor and the conduction loss of the inductor and power bridge is provided by the supply V_{in}. If $V_{out,fin}$ is lower than $V_{out,int}$, no work is done by V_{in}. Hence, the converter induced energy overhead is presented as the first term in Eq. 11, assuming the voltage upscaling and downscaling occur evenly. The other is the underclocking related loss, due to the mismatch of the supply voltage and clock frequency of the processor during the voltage scaling. Taking upsacling as an illustration, the clock frequency increases until the voltage scaling settles. During this period, the processor is supplied by an unnecessary high voltage. The underclocking related loss is estimated as the second term of Eq. 11, assuming that the output voltage scales linearly. The voltage scaling energy overhead of on-chip converters also benefits from the reduced filter capacitance.

$$E_{scale} = 0.5(C_{out}+C_{load})V_{in}|V_{out,fin}-V_{out,int}|+C_{load}min\{f_{sw,int},f_{sw,fin}\}\times\int_0^{T_{scale}}(V_{out}(t)^2-min\{V_{out,fin},V_{out,int}\}^2)\,\mathrm{d}t \tag{11}$$

The area consumption is also an important issue of the power delivery system design. In PowerSoC, we estimate the area consumption of the converters including the power bridge, the driver circuit, the control logic, and the inductor and capacitor of the output filter. The area of the transistors is determined by the channel length and width of the transistors, containing the area of the gate, drain and source. The channel length of transistors is related to the fabrication technology, and the channel width will be selected with the optimization technique proposed in Section II. The area of the drivers is derived by summarizing the areas of all the stages in the entire buffer chain and power bridge. The area consumption of the control logic per phase is estimated according to [3]. We assume that the output filter capacitor is implemented on-die with the deep-trench and thick oxide MOS capacitance, and the capacitance density is estimated referring to [13]. The on-package integrated inductor is selected to improve the power efficiency of the on-chip buck converter because of its high quality factor [3]. According to the products of Coilcraft [14], the ratio between the inductance and the area is derived.

B. Model of Power Delivery Network

In order to capture the overall property of the power delivery system, we also need to pay attention to the passive parasitics of the power delivery network, e.g. the parasitic resistance, capacitance and inductance

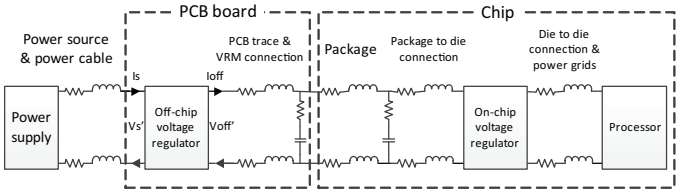

Fig. 4: Model of power delivery network with on-chip voltage regulators

of the printed board trace and package. A detailed model of the hybrid power delivery network with off-chip and on-chip voltage regulators is presented in Fig. 4. A ladder RLC network is utilized to capture the parasitics of the power delivery network. The on-board power supply is modeled as a fixed voltage source. The PCB board includes the PCB trace and off-chip decoupling capacitors. The power delivery network of the chip has the following components: the package and corresponding decoupling capacitors, package to die connection, die to die connection, and the lumped VDD and GND power grids of the processor. The package to die connection, e.g. C4 bumps, are modeled as lumped RL pairs that connect the on-chip voltage regulators to the power pins of the package. The on-chip voltage regulators then delivery the power to the processor through the die to die connection and the power grids of the processor.

II. Design exploration of power delivery systems

The analytical models of different components of the power delivery system are described including the buck converters and the parasitics of the power delivery network. Those properties of power delivery systems are determined by the selection of the converter design, e.g. channel width of the drivers and power bridge, inductance and the capacitance of the output filter. The conversion ratio of the converters in a multi-stage power delivery system is also considered. The intermediate voltage level tradeoff the power efficiency of different stages by affecting the conversion ratios. Generally speaking, the power efficiency of converters decreases as the conversion ratio increases. Hence, because of the wide design space, an optimization strategy is needed to find the optimal design variables. In PowerSoC, a method using convex optimization is adopted to find the optimal converter design that maximizes the power efficiency under the constraints of output ripple, transient response, area, etc. We utilize geometric programming (GP) to find the optimal design variables for different architectures of power delivery systems.

In the manual, the optimization strategy of the two-stage architecture combining both on-chip and off-chip converters is illustrated. In order to apply GP, the device models have to be compatible with GP. For the transistors of the power bridge, since they are in the linear region, R_{ds} is expressed as $\frac{k_{R_{ds}}}{W}$, where W is a width of a low-side device, and $k_{R_{ds}}$ is process and driver voltage dependent resistance per unit width at minimum gate length for low-side transistors of the bridge. The capacitance is modeled as $k_C \cdot W$, where k_C is process dependent parameters for switching capacitances multiplied by the accumulation of the channel width ratios of all the stages in the entire buffer chain of driver circuit and power bridge. The static power loss is expressed as $k_{P_{stat}} \cdot W$, and $k_{P_{stat}}$ is the process and supply voltage dependent leakage power per unit width, multiplied by the accumulation of the channel width ratios of the stages of driver circuit and power bridge. The switching power loss is assumed to be linearly scaled with the load current at the time of commutation [15]. It is expressed as $k_{P_{sw}} \cdot I_{out} \cdot f_{sw}$. $k_{P_{sw}}$ is the process and supply voltage dependent ringing loss per unit load current per cycle. For the transient voltage drop, the user-specified empirical factor α is estimated using the numerical fitting of SPICE simulations. It changes with the response time of the control strategy of converters. In the example, we adopt the voltage mode feedback control at switching frequencies of hundreds of MHz, and α is about 0.6, which is comparable to the results in [3]. Some of the device parameters are found for each process technology and voltage level by numerical fitting to SPICE simulation results of simple testing circuits. Some of the parameters, e.g. α and the channel width ratios of different stages of driver circuit and power bridge, are derived according to architectural selection of different buck converter designs. τ_e is the ratio between the resistance and

inductance of the inductors [5]. It is estimated according to the quality factor, which is assumed to be a constant within a certain range of switching frequency. The area consumption of different components of voltage regulators, e.g. the transistors, inductor and capacitor, are also included based on the selection of the voltage regulators, inductors and capacitors. $A_{driver,on}$ is the area consumption of the bridge and driver circuit per unit width of the power bridge, $A_{control,on}$ is the area overhead of the control logic per phase, and $A_{ind,on}$ and $A_{cap,on}$ are the area of the inductor and capacitor per unit inductance and capacitance accordingly. Besides the parameters of the voltage regulators, the impedance of power delivery network at the output of each voltage is also recorded in the configuration files.

The parameters of different components are derived based on the device and architecture selections of voltage regulator designs, and the results are recorded in the configuration files of voltage regulators and power delivery network. Besides the configuration of different components, the topology and temperature distribution of the power delivery system is required as the optimization input. The topology assignment of the voltage regulators is required to identify the connection relationship among different regulators. The supply voltage of the power delivery system V_{in}, the load distribution of power domains of the processor $V_{out,ij}$ and $I_{out,ij}$, and the intermediate voltage levels of the internal voltage regulators are provided. The temperature distribution of the power delivery system will adjust the device parameters of the transistor resistance, leakage current and the resistance of the inductor and power delivery network. The temperature coefficients of the parameters are also derived on the SPICE simulations of the simple teste circuit at different temperatures. The design spec constraints of each voltage regulator indicate the performance requirement and boundary of the design variables in the configuration files, e.g. the boundaries of design variables of different components, the maximum output ripples of regulators $V_{ripple,on,max}$ and $V_{ripple,off,max}$, the maximum transient voltage drop $V_{tr,on,max}$ and $V_{tr,off,max}$, and the area constraint of different stages $A_{on,max}$ and $A_{off,max}$.

The formulation of optimizing voltage regulators are described in Lines 3-11. The formulation is simplified as one-channel converter instead of the interleaved multiple phase one, because most of the properties of an interleaved converter, except the output ripple and control overhead, can be derived according to an equivalent one-channel converter with manipulating the design variables. Lines 3-5 define the boundaries of the multidimensional variable space of on-chip converters. The output stability constraints of each voltage regulator are shown in Line 7 and 8, e.g. the output ripple and transient voltage drop. The influence of the interleaving technique is shown in the calculation of the output ripple, and the corresponding power and area overhead of the control logic. The power consumption of each voltage regulator is calculated in Lines 9-11. The conduction loss of the impedance among different voltage regulators is included in Line 11, e.g. Z_{grid} indicates the resistance between voltage regulators and the processor. There are some modifications of the equations from equality to inequality in order to apply GP. However, the equality of the equations achieves, if the power losses are minimized. Similarly, the power consumption and design constraints of the voltage regulators in the other stage is shown in Line 12-20. The voltage regulator assignment of the power delivery system is shown in Line 21 and 22, indicating the relationship of the input and output voltage and current among different voltage regulators. The area overhead of voltage regulators in each stage is constrained in Line 23 and 24. The power efficiency of the entire power delivery system will be derived in Lines 25 and 26.

In most cases, the intermediate voltage levels are also important design variables in the power delivery system design. Selecting higher intermediate voltage levels will tradeoff among the power losses of the voltage regulators in adjacent stages. It will also reduce the conduction loss of power delivery network, by providing higher voltage level and reducing the supply current. We adopt the decomposition method to deal with it. Given a combination of intermediate voltage levels, the corresponding parameters of transistor model and inductor model become constant, and the formulation of the power delivery system design shown in Alg. 1 becomes a GP problem. The PowerSoC will generate a Matlab-based optimization script. The power efficiency of the power delivery system can be optimized using the existing Matlab-based convex solver of CVX [16]. The maximum power efficiencies for different combinations of intermediate voltage levels will be derived using the convex solver, and then be compared to find the optimal power

Algorithm 1 Optimization of the hybrid architecture

Require: parameters of different components, voltage regulator assignment, workload distribution of power domains, intermediate voltage levels, temperature distribution, boundaries of design variables of converters, design specs

minimize $\frac{P_{in}}{P_{out}}$

subject to

$W_{min,on} \leq W_{h/l,on,ij} \leq W_{max,on}, \forall i,j$

$f_{sw,on,min} \leq f_{sw,on,ij} \leq f_{sw,on,max}, \forall i,j$

$L_{ind,on,min} \leq L_{ind,on,ij} \leq L_{ind,on,max}, \forall i,j$

$\frac{W_{h,on,ij}}{W_{l,on,ij}} = \frac{\mu_{l,on,ij}}{\mu_{h,on,ij}}, \forall i,j$

$\frac{\Delta I_{ind,on,ij}}{8 f_{sw,on,ij}(C_{out,on,ij}+C_{load,ij})} \frac{0.25 V_{in,ij}}{D_{on,ij}(V_{in,ij}-V_{out,ij})} \frac{1}{N_{on,ij}^3} \leq V_{ripple,on,max}, \forall i,j$

$\alpha_{on} \cdot \Delta I_{out,tr,on,ij} \cdot \sqrt{\frac{L_{ind,on,ij}}{C_{out,on,ij}+C_{load,ij}}} \leq V_{tr,on,max}, \forall i,j$

$\frac{V_{out,ij}}{V_{in,ij}} \frac{R_{load,on,ij}+R_{ind,on,ij}+R_{pin,on,ij}+R_{ds,on,ij}}{R_{load,on,ij}} \leq D_{on,ij}, \forall i,j$

$\frac{(V_{in,ij}-V_{out,ij}) \cdot D_{on,ij}}{f_{sw,on,ij} \cdot L_{ind,on,ij}} = \Delta I_{ind,on,ij}, \forall i,j$

$C_{driver,on,ij} V_{in,ij}^2 f_{sw,on,ij} + (R_{ds,on,ij}+R_{ind,on,ij}+R_{pin,on,ij})(I_{out,ij}^2 + \frac{1}{12}\Delta I_{ind,on,ij}^2) + P_{stat,on,ij} + P_{sw,on,ij} + V_{in,ij} \cdot I_{control,on,ij} \cdot N_{on,ij} + Z_{grid,ij} \cdot I_{out,ij}^2 + V_{out,ij} \cdot I_{out,ij} \leq V_{in,ij} \cdot I_{on,ij}, \forall i,j$

$W_{min,off} \leq W_{h/l,off,j} \leq W_{max,off}, \forall j$

$f_{sw,off,min} \leq f_{sw,off,j} \leq f_{sw,off,max}, \forall j$

$L_{ind,off,min} \leq L_{ind,off,j} \leq L_{ind,off,max}, \forall j$

$\frac{W_{h,off,j}}{W_{l,off,j}} = \frac{\mu_{l,off,j}}{\mu_{h,off,j}}, \forall j$

$\frac{\Delta I_{ind,off,j}}{8 f_{sw,off,j} C_{out,off,j}} \frac{0.25 V_{in}}{D_{off,j}(V_{in}-V_{out,j})} \frac{1}{N_{off,j}^3} \leq V_{ripple,off,max}, \forall j$

$\alpha_{off} \cdot \Delta I_{out,tr,off,j} \cdot \sqrt{\frac{L_{ind,off,j}}{C_{out,off,j}}} \leq V_{tr,off,max}, \forall j$

$\frac{V_{out,j}}{V_{in}} \frac{R_{load,off,j}+R_{ind,off,j}+R_{ds,off,j}}{R_{load,off,j}} \leq D_{off,j}, \forall j$

$\frac{(V_{in}-V_{out,j}) \cdot D_{off,j}}{f_{sw,off,j} \cdot L_{ind,off,j}} = \Delta I_{ind,off,j}, \forall j$

$C_{driver,off,j} V_{drvier,off,j}^2 f_{sw,off,j} + (R_{ds,off,j}+R_{ind,off,j})(I_{off,j}^2 + \frac{1}{12}\Delta I_{ind,off,j}^2) + P_{stat,off,j} + P_{sw,off,j} + V_{driver,off,j} \cdot I_{control,off,j} \cdot N_{off,j} + (Z_{package}+Z_{PCB}) \cdot I_{off,j}^2 + V_{out,j} \cdot I_{off,j} \leq V_{in} \cdot I_{in,j}, \forall j$

$V_{in,ij} = V_{out,j}, \forall i,j$

$\sum_i^{M_j} I_{on,ij} \leq I_{off,j}, \forall j$

$A_{driver,on} \sum_i \sum_j (W_{h,on,ij}+W_{l,on,ij}) + A_{control,on} \sum_i \sum_j N_{on,ij} + A_{ind,on} \sum_i \sum_j L_{ind,on,ij} N_{on,ij}^2 + A_{cap,on} \sum_i \sum_j C_{out,on,ij} \leq A_{on,max}$

$A_{driver,off} \sum_j (W_{h,off,j}+W_{l,off,j}) + A_{control,off} \sum_j N_{off,j} + A_{ind,off} \sum_j L_{ind,off,j} N_{off,j}^2 + A_{cap,off} \sum_j C_{out,off,j} \leq A_{off,max}$

$\sum_j \sum_i (V_{out,ij} \cdot I_{out,ij}) = P_{out}$

$\sum_j I_{in,j} \cdot V_{in} \leq P_{in}$

efficiency of the system within the entire design space and the corresponding design variables.

III. PowerSoC file format

A. The parameter file

The parameter file of the voltage regulators ($param\_VR.txt$) describes the file names of the detailed parameters of different voltage regulators. The parameters of different voltage regulators are shown in Table I. The number of the parameters of the voltage regulators may changes for different kinds of voltage regulators. For example, the bulky buck converter usually have different supply voltages of the driver circuit

TABLE I: The format of the parameter file of voltage regulators.

$type$	the type of the voltage regulator with different parameters
N	the number of the parameters of the voltage regulator
$k_{R_{ds}}$ $(\Omega \cdot m)$	the resistance of the low-side transistor of power bridge per unit width
k_C $(F \cdot m^{-1})$	the switching capacitances of the driver circuit and power bridge per unit width of the bridge
$k_{P_{sw}}$ $(J \cdot A^{-1})$	the ringing power loss per unit load current per cycle
$k_{P_{stat}}$ $(W \cdot m^{-1})$	the leakage power of the driver circuit and power bridge per unit width of the bridge
τ $(H \cdot \Omega^{-1})$	the ratio between the resistance and inductance of the inductor
α	the user-specified empirical factor of the transient voltage drop estimation
$I_{control}$ (A)	the supply current of the control logic per phase
A_{driver} (m)	the area consumption of the driver circuit and power bridge per unit width of the bridge
A_{ind} $(m^2 \cdot H^{-1})$	the ratio between the area and inductance of the inductor
A_{cap} $(m^2 \cdot F^{-1})$	the ratio between the area and capacitance of the capacitor
$TC_{R_{ds},1}$ (K^{-1})	the temperature coefficient of the transistor resistance of power bridge
$TC_{R_{ds},2}$	the temperature coefficient of the transistor resistance of power bridge
$TC_{P_{stat},1}$ (K^{-1})	the temperature coefficient of the leakage power of the driver circuit and power bridge
$TC_{P_{stat},2}$	the temperature coefficient of the leakage power of the driver circuit and power bridge
TC_{ind}	the material identification of the inductor
$regulator\ \ assignment$	the number and indexes of the voltage regulators based on this design type

from the input voltage of the voltage regulators to reduce the power loss of the driver circuit. The thermal influence towards the on-state resistance and the static power of transistors and the material of the metal wires are also considered in our framework. The thermal influence of transistors is estimated based on SPICE simulations of the simple test circuits at different temperatures to estimate the relationship among on-state resistance, leakage current and temperature. The numerical fitting using linear regression is used, and the coefficients are given in the parameter file of the voltage regulators. The temperature coefficient of the inductor and power delivery network is estimated based on the selection of the used material, e.g. aluminium and copper. The parameter file of the power delivery network ($param\_PDN.txt$) indicates the parasitic impedance, material identification and temperature of the power delivery network at the output of each voltage regulator.

B. The configuration file

The configuration of a power delivery system includes the the configuration files of the multi-core processor, voltage regulator assignment and the design spec constraints. The configuration of the multi-core processor ($cfg\_proc.txt$) includes the number of the power domains of the multi-core processor, and each row represents the voltage level and current load of each power domain. Besides, it also includes the number and design space of the intermediate voltage levels in the order of voltage regulator indexes. In each row, it describes the number of the steps and lower and upper bound of the intermediate voltage levels. The configuration file of the voltage regulator assignment ($cfg\_PDS.txt$) indicates the connection relationship among different voltage regulators. It includes the number of the stage of the power delivery system. In each stage, the number of voltage regulators in this stage is described, and for each voltage regulator, the number and indexes of the successive voltage regulators or the on-chip power domains are described in each row. At last, the maximum area constraint of the voltage regulators in this stage is described. The configuration file of the design spec constraint ($cfg\_con.txt$) presents the boundary of the design variables and performance requirement of each voltage regulator in each row. It includes the lower bound and upper bound of the transistor channel width, the switching frequency, the inductance and capacitance of output filter of the voltage regulator and the temperature of the voltage regulators in each row. The default values of the design variable boundaries is assumed to be -1, which means there is no constraint of lower bound or upper bound of the design variables.

C. The output file

For the design space exploration of the power delivery system design, the output of the C++ based algorithm generates both a Matlab script $PDS\_optimization.m$ and a python script $PDS\_optimization.py$ to automatically solve the design optimization using the popular convex solver CVX [16] and $CVXOPT$ [17]. The optimization results based on CVX or $CVXOPT$ convex optimization, e.g. the design variables of voltage regulators and intermediate voltage levels, are recorded in the text file, $PDS\_optvals.txt$. It contains the optimum power efficiency of the entire power delivery system at the first line, and the optimization results of each voltage regulators in each session. For each voltage regulator designed using the buck converter topology, it describes the optimization results as follows: the input voltage level and current, the output voltage level and current, the power efficiency of the voltage regulator itself, the output ripple of output voltage, the transient voltage drop due to load step of 50% load current, the settling time of voltage scaling of 40% output voltage, the area consumption of voltage regulator, the channel width of the bridge, the switching frequency, the inductance of the inductor, the capacitance of the output capacitor and the number of interleaved phases. It provides not only the system-level properties, e.g. the power efficiency, output voltage stability and the area consumption, but also the detailed design of each voltage regulator, e.g. the switching frequency and the inductance and capacitance of the output filter. The detailed design of each voltage regulator can be used to further evaluate different design characteristics according to the requirements of users.

IV. USAGE INSTRUCTIONS

To compile the software, use g++ PowerSoC.cpp -o PowerSoC -lm To run the software, put the required input parameter and configuration files in the same folder and use ./PowerSoC to generate the Matlab script $PDS\_optimization.m$ and python script $PDS\_optimization.py$ To optimize the power delivery system design, run the Matlab script $PDS\_optimization.m$ using the Matlab with the CVX package installed, or run the python script $PDS\_optimization.py$ using the python with the $CVXOPT$ package installed

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