Thermal Analysis for 3D Optical Network-on-Chip Based on a Novel Low-Cost 6x6 Optical Router

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***Abstract*—We propose 3D mesh-based optical network-on-chip (ONoC) based on a novel low-cost 6x6 optical router, and quantitatively analyze thermal effects on the 3D ONoC. Evaluation results show that with the traditional thermal tuning technique using microheater, the average power efficiency of the 3D ONoC is about $2.7pJ/bit$, while chip temperature varies spatially between 55^oC and 85^oC. In comparison, a new technique using the optimal device setting can improve the average power efficiency to $2.1pJ/bit$. It is shown that in this particular case, the effectiveness of the two techniques is comparable. If we apply both techniques at the same time, the average power efficiency can be further improved to $1.3pJ/bit$.**

I. Introduction

As an emerging communication architecture for new-generation multiprocessor systems, optical networks-on-chip (ONoCs) can potentially offer ultra-high communication bandwidth and high energy efficiency. Recent developments in nanoscale silicon photonic devices substantially improve the feasibility of ONoCs [1]. However, as an intrinsic characteristic of photonic devices, thermal sensitivity is a potential issue in ONoC designs. As a result of thermo-optic effect, the temperature-dependent wavelength shifts in VCSEL (vertical cavity surface emitting laser) and silicon-based microresonator are found to be about 50-100$pm/^oC$ [2], [3]. As a widely used device in ONoCs, microresonator performs as a wavelength-selective optical switch or modulator. The thermal related wavelength variations will result in additional optical power loss. Besides, VCSEL power efficiency degrades at high temperatures [4]. Based on the system-level analytical ONoC thermal model proposed in [5], this work quantitatively studies the thermal effect on the 3D mesh-based ONoC based on a novel low-cost 6x6 optical router.

II. Thermal Analysis for 3D Mesh-Based ONoC

In this work, we present 3D mesh-based ONoC with a new 6x6 low-cost optical router (Figure 1) for dimension-order routing. In order to reduce the number of optical layers, we propose a floorplan (Figure 2) with routers in a single optical layer. The new 6x6 optical router is designed to passively route packets, and only one microresonator is required to be powered on when a packet makes a turn. Packets traveling between east and west, south and north, do not require to power on any microresonator. The passive routing feature of the new 6x6 optical router guarantees that the maximum number of switching stages in the 3D mesh-based ONoC with dimension-order routing is four. In order to minimize optical power loss, we further optimize the router to reduce the number of waveguide crossings.

To ensure that ONoCs function properly, a necessary condition is that the optical signal power received by a receiver should not be lower than the receiver sensitivity. This condition must hold, otherwise the bit error rate (BER) would increase significantly. We model the condition in Equation 1, assuming that the VCSEL and microresonators work at tempera-

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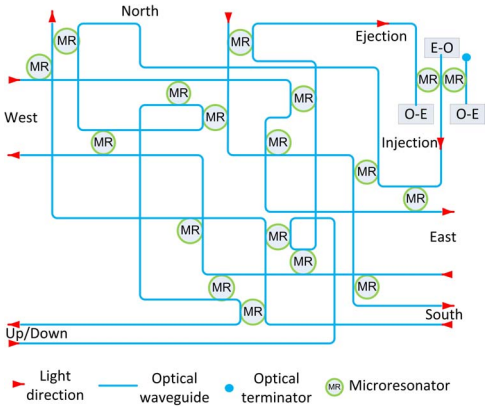

Fig. 1. 6x6 optical router for dimension-order routing

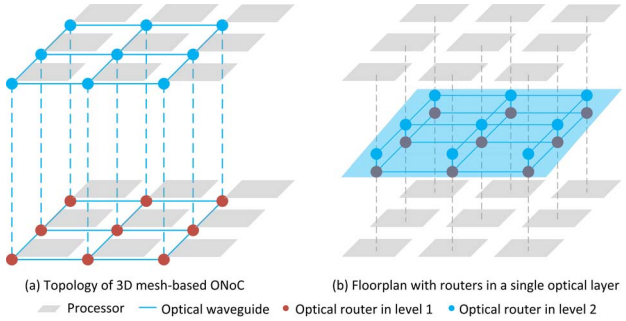

Fig. 2. Topology and floorplan of the 3D mesh-based ONoC

$$10log((I-\alpha-\beta(T_{VCSEL}-T_{th})^2)(\varepsilon-\gamma\cdot T_{VCSEL}))-\sum_{i=1}^{N}10log((\frac{2\kappa^2+\kappa_p^2}{2\kappa^2})^2\cdot(1+\delta^{-2}(\lambda_{VCSEL\_min}$$
$$+\rho_{VCSEL}(T_{VCSEL}-T_{min})-\rho_{MR}(T_{MR_i}-T_{min})-\lambda_{MR\_min})^2))-L_{WG}\geq S_{RX} \quad (1)$$

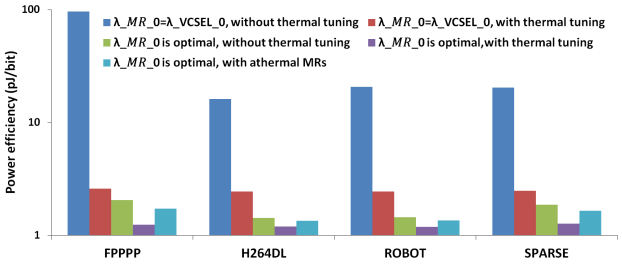

Fig. 3. Power efficiency of 3D 8x8x2 mesh-based ONoC under different MPSoC applications, $T_{max}=85^oC$

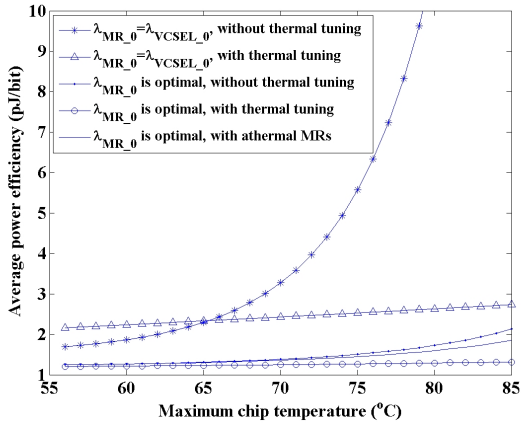

Fig. 4. Average power efficiency of 3D 8x8x2 mesh-based ONoC with different configurations

ture T_{VCSEL} and T_{MR_i}, respectively [5]. The temperature-dependent wavelength shift of VCSEL and microresonators are denoted by ρ_{VCSEL} and ρ_{MR}. The first term of Equation 1 is the output power of the VCSEL driven by current I which is above the threshold I_{th}. The second term is summation of optical power loss due to N switching stages of microresonators, assuming that the 3-dB bandwidth of microresonators is 2δ. L_{WG} is the waveguide propagation loss in the link, and S_{RX} is the sensitivity of the receiver.

Two traditional techniques have been proposed to compensate the temperature-dependent wavelength shift for microresonators, including active thermal tuning with local microheaters and passively temperature-compensated athermal microresonators [6], [7]. Besides the use of optimized optical routers (Figure 1) with minimized number of switching stages, we propose a new passive temperature compensation technique using the optimal device setting to improve the power efficiency of ONoCs under thermal variations [5].

We quantitatively evaluate the power efficiency of the 3D ONoC under different combinations of device setting and low-temperature-dependence techniques. Figure 3 shows the power efficiency of the 3D 8x8x2 mesh-based ONoC under different MPSoC applications, assuming that the maximum chip temperature T_{max} reaches 85^oC. Figure 4 shows the average power efficiency of the 3D 8x8x2 mesh-based ONoC under different maximum temperature T_{max}. We assume that the minimum chip temperature is 55^oC, the 3-dB bandwidth of microresonators is 3.1nm, and the receiver sensitivity is $-14.2dBm$ for a BER of 10^{-12} [8]. If the initial microresonator resonance wavelength λ_{MR_0} is equal to λ_{VCSEL_0}, the average communication power efficiency is $25pJ/bit$ when the maximum chip temperature reaches 85^oC. It can be improved to about $2.7pJ/bit$ by applying the traditional thermal tuning technique with microheater, assuming that the tuning efficiency is $3.5mW/nm$ [6]. The new technique using the optimal device setting can improve the average power efficiency to $2.1pJ/bit$ [5]. It is shown that in this particular case, the effectiveness of the two techniques is comparable. If the two techniques are applied at the same time, the average power efficiency can be further improved to $1.3pJ/bit$. If we apply the optimal device setting with athermal microresonators, the average power efficiency is about $1.8pJ/bit$. Since thermal tuning and athermal microresonators could impose high fabrication cost, the new technique using the optimal device setting without thermal tuning is also an alternative solution in this particular case.

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