A Novel Low-Waveguide-Crossing Floorplan for Fat Tree Based Optical Networks-on-Chip

Zhehui Wang†, Jiang Xu†, Xiaowen Wu†, Yaoyao Ye†, Wei Zhang‡,
Weichen Liu†, Mahdi Nikdast†, Xuan Wang†, Zhe Wang†
†Department of Electronic and Computer Engineering, The Hong Kong University of Science and Technology
‡School of Computer Engineering, Nanyang Technological University, Singapore
Email: {zhehui,jiang.xu}@ust.hk, zhangwei@ntu.edu.sg

***Abstract*—Optical network-on-chip (ONoC) can be used as the communication backbone for high performance chip multiprocessors (CMPs). Fat tree based ONoC shows high throughput, small delay and low power consumption. However, the traditional floorplan design of fat tree based ONoC has a large number of waveguide crossings because of the fat tree topology. In this paper, we present an optimized floorplan with the least number of waveguide crossings that has been reported. The average number of waveguide crossings per optical path in the optimized floorplan is 87% less than that in traditional floorplan for a 64-core CMP. We also find the optimal aspect ratio of cores to minimize the end-to-end delay. These work could help to ease the physical implementation of fat tree based ONoC for CMP.**

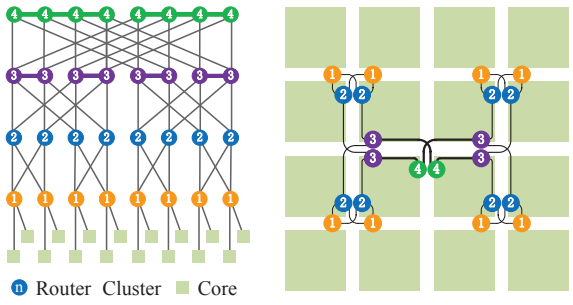
I. Introduction

The development of on-chip optical components make optical network-on-chip (ONoC) a promising communication system for chip multiprocessors (CMPs) [1], [2]. ONoC can be classified by different topologies. Regular topologies used by ONoCs include mesh, torus, ring (1-dimension torus), fat tree, *etc* [3], [4], [5]. Fat tree based ONoC shows high throughput, small delay and low power consumption [6]. The floorplan of fat tree based ONoC plays an important role in network performance and cost. A large number of waveguide crossings will attenuate signals and introduce crosstalk noise [7]. Besides, the end-to-end delay in fat tree based ONoC will be increased by long interconnects. These problems also limit the scalability of fat tree based ONoC because its power and area cost will worsen significantly when the network size increases. In this paper, we present an optimized floorplan for fat tree based ONoC with less crossings and shorter interconnects. We also find the optimal aspect ratio of cores in CMP using fat tree based ONoC.

II. Optimized Floorplan

Fig. 1(a) shows the fat tree based ONoC. It consists of optical routers and interfaces to cores, which are connected by optical interconnects. Routers are able to switch optical signals from one port to another. Routers can be divided into different levels. Cores are connected to fat tree based ONoC by optical-electronic and electronic-optical interfaces. The electronic signals sent by source cores are converted into optical signals, transmitted through ONoC, and converted back to electronic signals for destination cores. Each interconnect is bidirectional and is made up of two optical waveguides. Packets transmitted in fat tree based ONoC will go through three stages. In the first stage, the packets from the source cores climb the tree from low-level routers to high-level

This work is partially supported by RPC11EG18.



(a) Topology (b) Floorplan

Fig. 1. The fat tree topology and its traditional floorplan for 16-core CMP fat tree based NoC

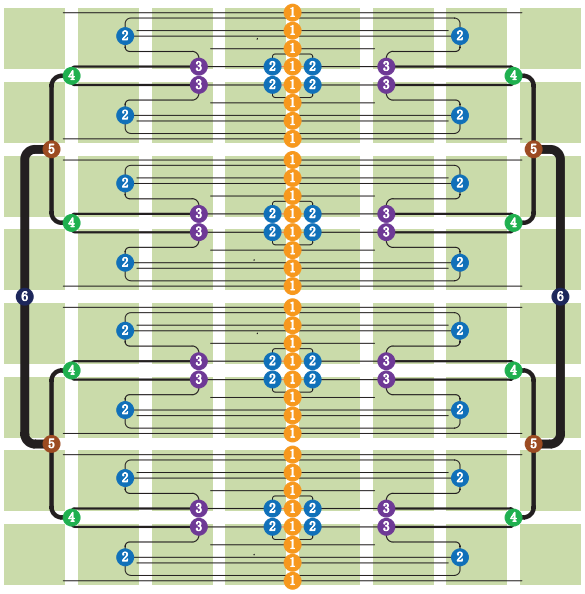


Fig. 2. The optimized floorplan of fat tree based ONoC for 64-core CMP

routers. Each router will choose one port to move the packet upward based on a routing algorithm. In the second stage, the packets arrive at routers, which are the common ancestors of the source cores and destination cores. Finally, the packets move downward from high-level routers to low-level routers and reach the destination cores.

Fat tree based ONoC can be fabricated on a separate optical layer, which could be stacked onto electronic layers for cores. Traditional floorplan design favorites H-tree, and it is shown in Fig. 1(b). Multiple routers at the same level are grouped into clusters for floor planning purposes. Clusters also have levels, which are the same with the levels of inside routers. Clusters at level 1 and level 2 have only one router, and the other level clusters have two or more than two routers. H-tree based floorplan has a large number of waveguide crossings, which cause large insertion loss and crosstalk noise. We propose an optimized floorplan in Fig. 2, whose router clusters are the same as those in the traditional floorplan. Our floorplan for fat tree based ONoC has the least number of crossings that has been reported. Another important characteristic in the floorplan is the traversal distance of a signal, which affects end-to-end delays in fat tree based ONoC. We find that the traversal distance is related to the aspect ratio of cores, and an optimal core aspect ratio is existed to minimize the traversal distance.

III. Quantitative Result and Analysis

We analyze the optimized fat tree ONoC floorplan for 64-core CMP. The number of waveguide crossings on the path between any two cores in the traditional floorplan and the optimized floorplan are shown in Fig. 3. Cores are indexed, and each optical path can be distinguished by the combination of a source core index and a destination core index. Cores on a CMP are indexed in a zigzag fashion, and neighboring cores have close indices. The number of crossings on each path is shown by different colors. In both floorplans, paths between neighboring cores have less crossings than paths between faraway cores. Half paths in the traditional floorplan have 166 crossings. On the other hand, all paths in the optimized floorplan have less than 22 crossings. The average number of waveguide crossings per optical path in the optimized floorplan is 87% less than that in the traditional floorplan. This analysis shows that our optimized floorplan can significantly reduce the number of waveguide crossings.

We also analyze the traversal distance of the fat tree based ONoC for 64-core CMP. The relationships between the average traversal distance per optical path and the aspect ratio of cores for the two floorplans are plotted in Fig. 4. The chip area, which is the total area of 64 cores, is assumed to be a constant. Therefore, the traversal distance can be represented by its ratio to the square root of chip area. The average traversal distances of both floorplans are between one to three times of the square root of chip area when the aspect ratio is close to one. We find that each floorplan has an optimal aspect ratio of cores, which can minimize the average traversal distance. For the traditional floorplan, the average traversal distance is 0.97

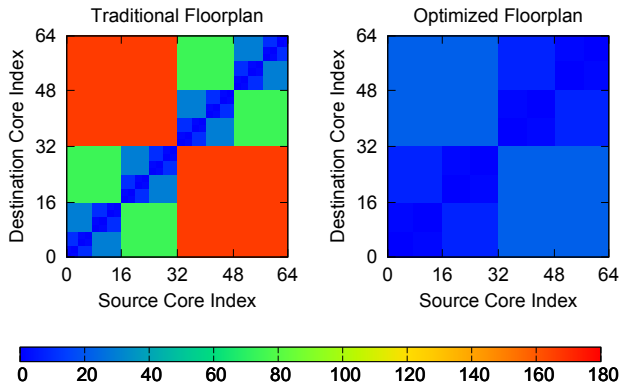


Fig. 3. The number of waveguide crossings on each optical path between any two cores in the traditional floorplan and optimized floorplan

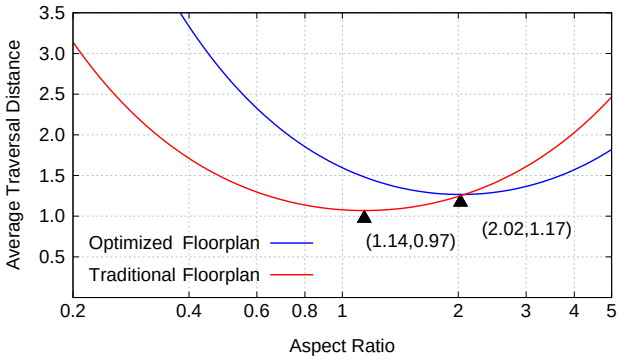


Fig. 4. Relationships between average traversal distance per optical path and aspect ratio of cores in 64-core CMP with fat tree based ONoC

with optimal aspect ratio 1.14. For the optimized floorplan, the average traversal distance is 1.17 with optimal aspect ratio 2.02. Since the traditional floorplan uses H-tree, it has the minimum Manhattan distance for each optical path. While our optimized floorplan significantly reduces the waveguide crossings, and only marginally increases the average traversal distance, compared to the traditional floorplan.

References

[1] B. Little, J. Foresi, G. Steinmeyer, E. Thoen, S. Chu, H. Haus, E. Ippen, L. Kimerling, and W. Greene, "Ultra-compact si-sio2 microring resonator optical channel dropping filters," *Photonics Technology Letters, IEEE*, vol. 10, no. 4, pp. 549 –551, apr 1998.

[2] S. P. M. L. Q. Xu, B. Schmidt, "Micrometre-scale silicon electro-optic modulator," in *Nature*, vol. 435, no. 7040, 2005.

[3] C. E. Leiserson, "Fat-trees: universal networks for hardware-efficient supercomputing," *IEEE Transactions on Computers*, vol. 34, pp. 892–901, Oct. 1985.

[4] J. Balfour and W. J. Dally, "Design tradeoffs for tiled cmp on-chip networks," in *Proceedings of Supercomputing*, 2006, pp. 187–198.

[5] S. Ohring, M. Ibel, S. Das, and M. Kumar, "On generalized fat trees," in *Parallel Processing Symposium*, apr 1995, pp. 37 –44.

[6] H. Gu, J. Xu, and W. Zhang, "A low-power fat tree-based optical network-on-chip for multiprocessor system-on-chip," in *Design, Automation Test in Europe Conference Exhibition*, 2009, pp. 3 –8.

[7] Y. Xie, M. Nikdast, J. Xu, W. Zhang, Q. Li, X. Wu, Y. Ye, X. Wang, and W. Liu, "Crosstalk noise and bit error rate analysis for optical network-on-chip," in *Design Automation Conference*, june 2010, pp. 657 –660.