A Holistic Modeling and Analysis of Optical–Electrical Interfaces for Inter/Intra-chip Interconnects

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***Abstract*— With the fast development of inter/intra-chip optical interconnects, the gap between the data rates of electrical interconnects and optical interconnects is continuously increasing. Electrical–optical (E-O) interfaces and optical–electrical (O-E) interfaces are a pair of components that convert data between parallel electrical interconnects and serial optical interconnects. This paper holistically models and analyzes E-O and O-E interfaces in terms of energy consumption, area, and latency. Traditional interfaces, where data are converted between parallel and serial ports by serializers and deserializers (SerDes), are studied. A new type of E-O and O-E interface, which serializes and deserializes data by optical weaving technologies, are proposed alongside. Traditional interfaces will become a bottleneck for the further development of optical interconnects in the near future because of the high energy consumption and large area of SerDes necessitating new technologies. Our analysis shows that optical weaving interfaces have a better overall performance than traditional interfaces. For example, if there are 64 parallel electrical interconnects and four optical wavelengths, optical weaving interfaces can achieve a 81.6% improvement in energy consumption and a 40.8% improvement in area, compared with traditional interfaces.**

***Index Terms*— Optical interconnect, optical resonators, performance analysis, time-division multiplexing (TDM).**

I. Introduction

TODAY, the data rate of optical signals in a single wavelength is typically in the scale of tens of gigahertz [1]. With the fast development of optical technologies, the difference in data rate between electrical interconnects and optical interconnects is continuously increasing [2]. Therefore, electrical–optical (E-O) interfaces and optical–electrical (O-E) interfaces have become important components in high-speed inter/intra-chip interconnects. The E-O interface converts data from parallel electrical interconnects to serial optical interconnects, and the O-E interface converts data from serial optical interconnects back to parallel electrical interconnects. Traditionally, parallel data are converted to serial data by serializers, and serial data are converted back to parallel data by deserializers. These components work like funnels on both sides of the interconnects.

In traditional E-O interfaces and O-E interfaces, it is difficult to improve the speed of serializers and deserializers (SerDes) and decrease their power consumption or area at the same time [2]. In order to increase data rates, traditional high-speed SerDes consist of multiple stages of multiplexers or demultiplexers. Therefore, there are a large number of latches in SerDes. Most of these latches work as registers and clock dividers, which consume a large proportion of the power and area. Studies show that when the parallel-to-serial ratio (defined as the ratio between the number of electrical interconnects and the number of optical wavelengths in an E-O interface) is increased, the power consumption and area of high-speed SerDes increase superlinearly [3]. Therefore, the serializers in traditional E-O interfaces and deserializers in traditional O-E interfaces will become a bottleneck of inter/intra-chip optical interconnects in the near future. To specify their mechanisms, the traditional interfaces are called electrical funneling interfaces in this paper.

Fundamentally, E-O and O-E interfaces are time-division multiplexing (TDM) systems. In TDM designs, the time domain of the optical interconnect is divided into multiple time slots with fixed length, one for each electrical interconnect. A popular example is the optical TDM (OTDM) system, which is widely used in telecommunications networks [4], [5]. In OTDM systems, parallel optical signals are serialized by a group of modulators. Each of the modulators is delayed by a fraction of the clock period, and data from the parallel electrical interconnects are optically weaved to a serial optical fiber by the group of modulators. We propose a mechanism called optical weaving interfaces, which are able to serialize and deserialize using O-E SerDes.

In the optical weaving E-O and O-E interfaces, an array of microresonators are implemented along the waveguide to multiplex or demultiplex optical signals directly. The active time of each microresonator is delayed by a fixed amount

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of time so that parallel electrical signals can be optically weaved to the optical waveguide. These new interfaces using optical weaving technologies have many advantages over traditional electrical funneling interfaces. For instance, the number of latches is effectively reduced by this new technology, especially when the parallel-to-serial ratio is very high [6]. In addition, optical weaving interfaces are compatible with traditional electrical funneling interfaces. For example, optical weaving E-O interfaces can work with electrical funneling O-E interfaces as pairs.

In this paper, the performance of both electrical funneling and optical weaving E-O interfaces and O-E interfaces is analyzed under different data rates, technologies, and parallel-to-serial ratios. Assumptions are made based on state-of-the-art technologies. A general configuration of inter/intra-chip optical interconnects, which consists of a customized number of electrical data sources and a customized number of optical wavelengths, is also analyzed. In the general configuration, multiple pairs of E-O interconnects and O-E interfaces work together on both sides of the optical interconnects. In addition, the performances of interconnects with electrical funneling interfaces and optical weaving interfaces are quantitatively analyzed and compared.

The rest of this paper is organized as follows. Section II gives a survey of E-O/O-E interfaces and SerDes for high-speed inter/intra-chip interconnects. Section III introduces the architectures of traditional electrical funneling interfaces, while Section IV models the two types of interfaces and studies the architectures of optical weaving interfaces. Section V quantitatively analyzes and compares the performance of inter/intra-chip interconnects with electrical funneling interfaces and those with optical weaving interfaces. Finally, Section VI concludes this paper.

II. Related Work

Many works have focused on improving the throughputs of optical interconnects. Some of these works have used wavelength-division multiplexing (WDM) technology. Manipatruni *et al.* [7] implemented an interconnect with four microresonator modulators. In their system, each of the modulators has a 12.5-Gbit/s modulation capability. Also, Li *et al.* [8] implemented a microresonator-based inter/intra-chip interconnect, in which parallel electrical signals are converted into serial signals by serializers. TDM is also an important technology for fiber-based optical interconnects in telecommunications. Spirit *et al.* [4] proposed generalized models for OTDM transmission system. In this model, each modulated signal is delayed by a fixed amount of time. Microresonators have been used to multiplex or demultiplex optical signals. Poon *et al.* [9] proposed a cascaded microresonator-based matrix switch for optical interconnects. This matrix switch can function as an optical multiplexer or demultiplexer. Wang *et al.* [10] made a holistic analysis of the energy consumption, bandwidth density, and latency. Finally, pluggable optical transceivers are developed around the world, which use WDM/TDM technologies to design interfaces between parallel electrical interconnects and serial optical interconnects [11]–[13].

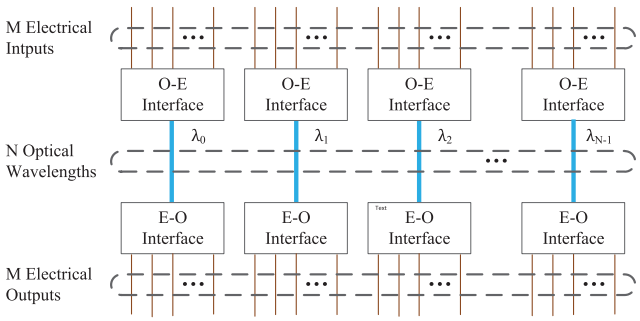

Fig. 1. OI(M, N) converts M electrical inputs into N optical wavelengths and converts them back to M electrical outputs.

The performance of interfaces for inter/intra-chip interconnects is related to the architectures of SerDes. In traditional electrical funneling interfaces, serializers are based on multistage multiplexers, which have high date rates and complicated circuits. Tsai *et al.* [14] proposed a low gate-count pipeline topology for serial interconnects, which reduces power consumptions and areas. Park *et al.* [15] designed a wide-input-range serializer, in which the first stage of the multiplexer is implemented with a shift-register architecture for chip area reduction. Wong and Chen [6] designed a 2.5-Gbit/s serializer, and to reduce the area, parallel data are converted into serial data by multiphase clock signals directly. Kehrer and Wohlmuth [3] implemented a 4:1 serializer using current-mode logic (CML). The use of CML is essential for low power consumption while achieving maximum speed. Tobajas *et al.* [16] implemented a multistage 1:32 deserializer using emitter-coupled logic (ECL). In order to reduce power consumptions, the high-speed circuits were designed with bipolar ECL structures.

III. Background

In this section, a general configuration of interconnects with a customized number of electrical data sources and wavelengths is modeled. Traditional electrical funneling E-O interfaces and O-E interfaces, which are able to convert data between parallel electrical and serial optical interconnects in inter/intra-chip communications, are also introduced.

A. OI(M, N) Configuration

The general configuration of inter/intra-chip optical interconnects consists of M electrical inputs/outputs and N optical wavelengths. It is shown in Fig. 1. Multiple optical wavelengths can be transmitted by a single waveguide or multiple waveguides [2]. On both sides of the optical interconnects, there are N pairs of E-O interfaces and O-E interfaces. It is assumed that the parallel-to-serial ratio in each pair of interfaces is the same as that of others. Hence, the parallel-to-serial ratio is M/N. There are multiple combinations of M and N. When N equals M, each electrical input/output is directly mapped to each optical wavelength, and it is unnecessary to design SerDes in the E-O and O-E interfaces. When N decreases from N to 1, the parallel-to-serial ratio of interfaces increases. When N equals 1, M electrical inputs/outputs

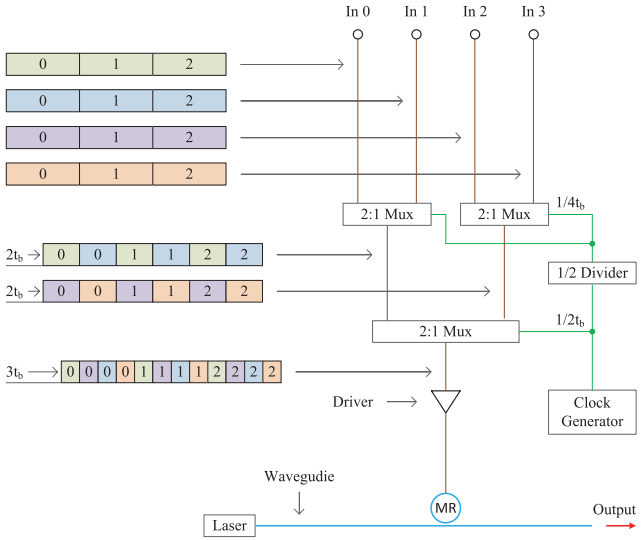

Fig. 2. Electrical funneling E-O interface funnels data from multiple electrical channels into one optical channel by one serializer.

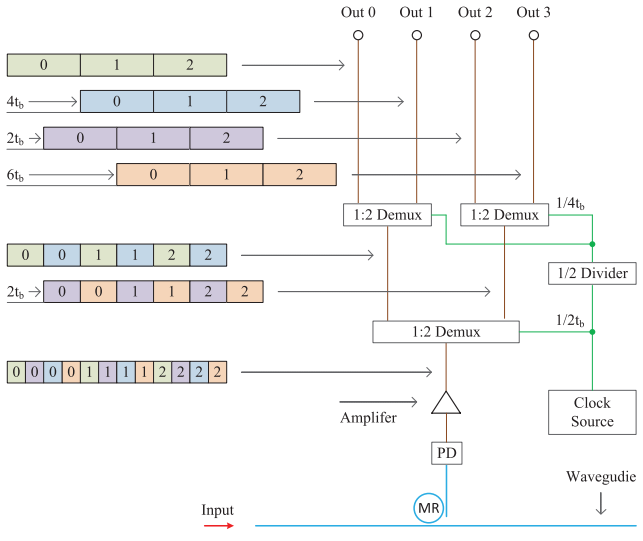

Fig. 3. Electrical funneling O-E interface converts data from one optical channel to multiple electrical channels by one deserializer.

are mapped to M optical wavelengths. SerDes in E-O and O-E interfaces will have the highest parallel-to-serial ratios. The general configuration of inter/intra-chip optical interconnects is denoted by OI(M, N). We focus on two types of E-O interfaces and O-E interfaces: traditional electrical funneling interfaces and optical weaving interfaces. Assuming the optical interconnects have the same types of E-O interfaces and O-E interfaces, two types of OI(M, N) are studied: electrical funneling OI(M, N) and optical weaving OI(M, N). In Section V, their performance is quantitatively analyzed and compared.

B. Electrical Funneling E-O Interface

Traditional E-O interfaces convert parallel electrical signals into serial optical signals. In this paper, they are called electrical funneling E-O interfaces because parallel data are funneled to optical interconnects by serializers. The structure of a 4:1 electrical funneling E-O interface, which consists of a multistage tree multiplexer, a clock generator, a laser source, a driver, and a modulator, is shown in Fig. 2. There are four parallel electrical input signals, which are nonreturn-to-zero (NRZ) coded. The data rate of each input signal is $1/4t_b$, where $4t_b$ is the bit time of the input signals. The tree-based multiplexer consists of two stages of 2:1 multiplexer blocks [17]. The first stage works on a $1/4t_b$ frequency and converts four parallel signals into two parallel signals. The second stage works on a $1/2t_b$ frequency and converts the two parallel signals into one serial signal. Clock generator modules are typically implemented by phase-locked loops (PLLs) [18], and here, high-frequency clock signals are converted into low-frequency clock signals by 1/2 dividers. The multiplexer output data rate is $1/t_b$. The output is connected to the driver, which outputs enough current to drive the optical modulator. One microresonator is implemented along the waveguide to modulate the optical signals. The radius of that microresonator is particularly designed so that its resonance wavelength equals the wavelength of optical light. Similar to the parallel electrical inputs, the serial optical outputs are also NRZ coded. After time t_b, one bit of information is outputted.

In optical WDM systems, signals with different wavelengths are transmitted in one waveguide [19]. In the traditional electrical funneling OI(M, N), there are N electrical funneling E-O interfaces, and each of them has M/N parallel inputs. An array of N microresonators are implemented along the waveguide to modulate N different optical wavelengths. Each microresonator has a unique resonance wavelength and belongs to one of the E-O interfaces. In a basic multiplexer block, the output signal is delayed. After multiple stages of multiplexer blocks, the latencies of the serial optical outputs are $(M/N - 1) \cdot t_b$, as shown in Fig. 2. Because of process and temperature variations, the resonate wavelengths of the microresonators do not precisely match the wavelengths of the laser sources. This means that the modulation depths of the microresonators will be decreased, and it becomes difficult to detect optical signals. Tuners are therefore integrated on microresonators to adjust the resonance wavelengths [19].

C. Electrical Funneling O-E Interface

Traditional O-E interfaces convert serial optical signals into parallel electrical signals, and serial data from optical interconnects are converted into parallel data by deserializers. The structure of a 1:4 electrical funneling O-E interface, which consists of a multistage tree demultiplexer, a clock source, a filter, a photodetector, and an amplifier, is shown in Fig. 3. The inputs of the serial optical signals are NRZ coded with data rate $1/t_b$. The tree-based demultiplexer consists of two stages of 1:2 multiplexer blocks [20]. The first stage works on a $1/2t_b$ frequency and converts one serial signal into two parallel signals. The second stage works on a $1/4t_b$ frequency and converts two parallel signals into four parallel signals. In optical inter/intra-chip interconnects, clock signals can be extracted from optical signals directly, or be transmitted by

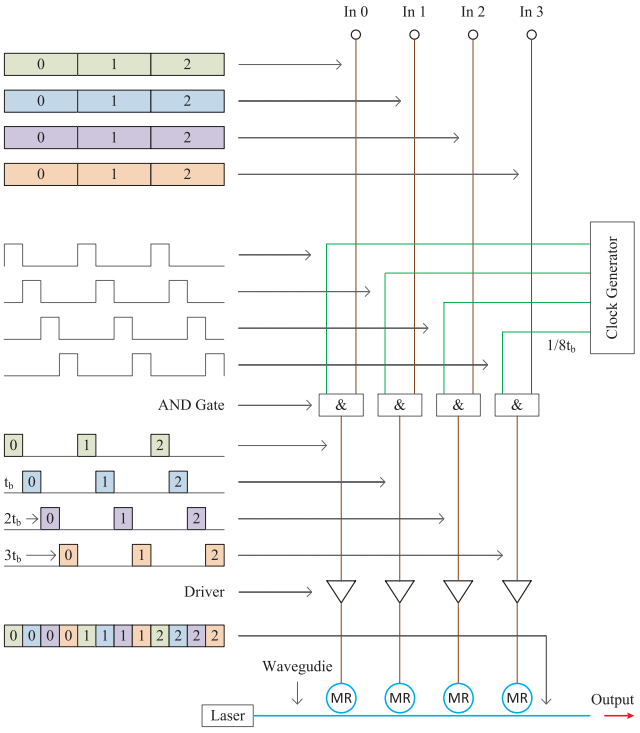

Fig. 4. Optical weaving E-O interface weaves data from multiple electrical channels into one optical channel by an array of microresonators.

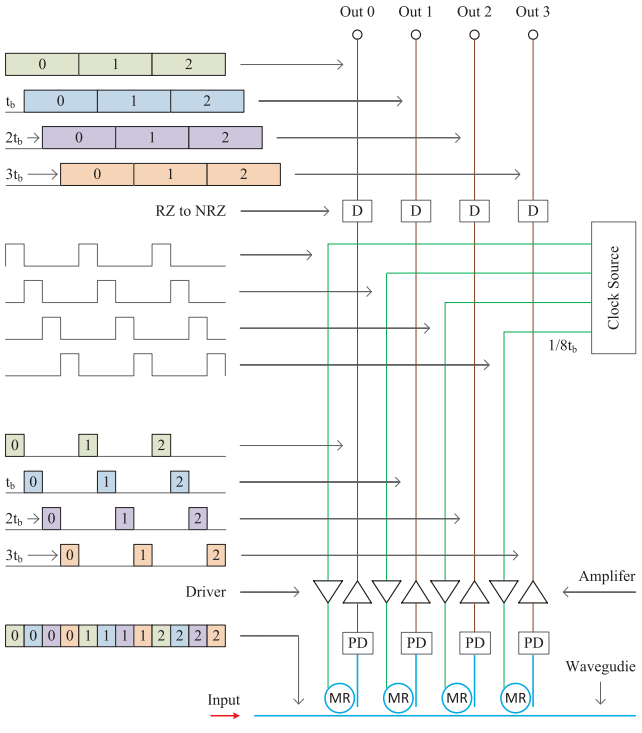

Fig. 5. Optical weaving O-E interface converts data from one optical channel to multiple electrical channels by an array of microresonators.

independent optical wavelengths. The clock source module is able to recover clock signals. High-frequency clock signals are converted into low-frequency clock signals by 1/2 dividers. The demultiplexer output data rates are $1/4t_b$. One microresonator is implemented along the waveguide to filter optical signals, whose resonance wavelength equals the wavelength of optical light. The parallel electrical outputs are also NRZ coded. After time $4t_b$, one bit of information is outputted.

In the electrical funneling OI(M, N), there are also N electrical funneling O-E interfaces, and each of them has M/N parallel outputs. An array of N microresonators are implemented along the waveguide to filter the N different optical wavelengths. In optical WDM systems, each microresonator has a unique resonance wavelength and belongs to one of the O-E interfaces. In a basic demultiplexer block, one of the two parallel output signals is delayed. After multiple stages of demultiplexer blocks, the latencies of M/N parallel electrical outputs range from 0 to 2 $(M/N-1)\cdot t_b$, as shown in Fig. 3. The average latency of the electrical funneling O-E interface is $(M/N-1)\cdot t_b$. To adjust the resonance wavelengths, tuners are integrated on the microresonators.

IV. E-O and O-E Interfaces' Modeling

In this section, the performances of components in E-O interfaces and O-E interfaces are analyzed and modeled in terms of power consumption and area. Details of optical weaving E-O and O-E interfaces are discussed. An array of microresonators are implemented along the waveguide to multiplex or demultiplex optical signals directly.

A. Optical Weaving E-O Interface

Optical weaving E-O interfaces convert parallel electrical signals into serial optical signals. The structure of a 4:1 optical weaving E-O interface, which consists of an AND gate, a clock generator, a laser source, a driver, and a modulator, is shown in Fig. 4. The four parallel electrical inputs are NRZ coded with data rate $1/4t_b$ and are converted into serial data by TDM systems. The output frequencies of the clock generators in the optical weaving interfaces are $1/8t_b$, one-fourth of the frequencies in electrical funneling interfaces. The clock generator module has four outputs, which are equally phase shifted by $\pi/2$. Each clock signal is used to control one of the electrical input signals by a gate. Therefore, the parallel signals are enabled by turns. Different from electrical funneling interfaces, there are four microresonators implemented along the waveguide to modulate the optical signals. These microresonators are designed to modulate the same optical wavelength. In OTDM systems, they will not interfere with each other because, at any time, only one of the microresonators is activated. The output optical signals have the same waveform as electrical funneling interfaces, which are also NRZ coded.

In the optical weaving OI(M, N), each E-O interface has M/N parallel inputs, and an array of M microresonators are implemented along the waveguide to modulate the N different optical wavelengths. All M microresonators belong to the N interfaces. Each interface has M/N microresonators to modulate the same wavelength. Gates in optical weaving interfaces do not have latencies. Because the first bit of electrical input 0 will be converted into serial optical

signals immediately. Here, the latencies of the serial optical outputs are zero, as shown in Fig. 4. Due to process and temperature variations, the resonance wavelengths of the microresonators will drift. In order to align them with the wavelength of the laser source, tuners are integrated on the microresonators.

B. Optical Weaving O-E Interface

Optical weaving O-E interfaces convert serial optical signals into parallel electrical signals. The structure of a 1:4 optical weaving O-E interface, which consists of a driver, a clock source, a filter, a photodetector, an amplifier, and a converter, is shown in Fig. 5. The serial optical inputs are NRZ coded with data rate $1/t_b$, and they are converted into parallel data by TDM systems. The clock source module recovers clock signals, and it has four outputs, which are equally phase shifted by $\pi/2$. In the optical weaving interfaces, there are four microresonators implemented along the waveguide to filter the optical signals. They are designed to have the same resonance wavelength, which equals the wavelength of the optical signals. Different from the filters in electrical funneling interfaces, the filters in the optical waving interface are not passive. Each of them is driven by one of the clock signals. At any time, only one of the microresonators is activated, and optical signals are filtered to the receiver module by that microresonator. The parallel output signals are return-to-zero (RZ) coded. To have the same waveform as that of the electrical funneling interfaces, an RZ-to-NRZ converter is connected to each electrical output.

In the optical weaving OI(M, N), each O-E interface has M/N parallel outputs, an array of M microresonators are implemented along the waveguide to filter the N different optical wavelengths, and all M microresonators belong to the N interfaces. Each interface has M/N microresonators to filter the same wavelength. In the optical weaving O-E interface, signals in some electrical outputs will be delayed because of their places on the serial optical signals. The latencies of the M/N parallel electrical outputs range from 0 to $(M/N-1)\cdot t_b$, as shown in Fig. 5. The average latency of the optical weaving O-E interface is $(M/2N - 1/2) \cdot t_b$. Tuners are integrated on the microresonators to adjust the resonance wavelengths.

C. Multiplexer Block

In electrical funneling E-O interfaces, the multiplexer blocks are important components that select one of several input signals and forward the data from the selected input port to the output port. The basic multiplexer block, which has two inputs and one output, is shown in Fig. 6(a). To store the bits of information during each clock cycle, three latches are implemented [2]. Clock signals are used to select the input signals, and in this design, input 0 is selected when the clock signal is low, and input 1 is selected when the clock signal is high. Multiplexer blocks in different stages are connected to different frequencies. A 1/2 clock divider is implemented in each stage to provide clock signals with different speeds. In optical weaving E-O interfaces, there is an array of gates, which enable one of several input signals based on phase-shifted clock signals. Examples of output waveforms of drivers in the two types of E-O interfaces are shown in Fig. 8.

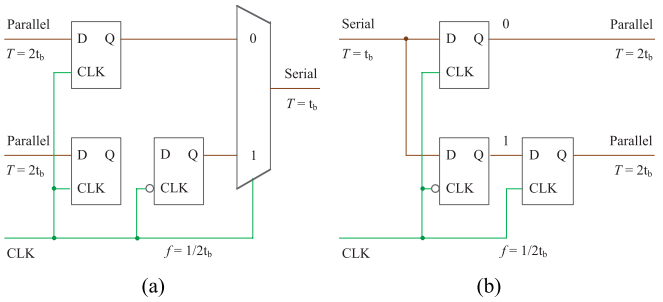

Fig. 6. (a) Basic multiplexer block converts data from two parallel channels into one serial channel. (b) Basic demultiplexer block converts data from one serial channel into two parallel channels.

TABLE I

CURRENT BREAKDOWN OF MULTIPLEXER BLOCKS (UNIT CURRENT I_0 IS DEFINED IN SECTION IV-C)

Component	4:1 SER	8:1 SER	16:1 SER	R:1 SER
Multiplexer	2	3	4	$log_2 R$
Latch	6	9	12	$3log_2 R$
Clock Divider	2	3	3.5	$4 - 8/R$
Total (I_0)	10	15	19.5	$\approx 5log_2 R$

TABLE II

CURRENT BREAKDOWN OF DEMULTIPLEXER BLOCKS (UNIT CURRENT I_0 IS DEFINED IN SECTION IV-C)

Component	1:4 DES	1:8 DES	1:16 DES	1:R DES
Latch	6	9	12	$3log_2 R$
Clock Divider	2	3	3.5	$4 - 8/R$
Total (I_0)	8	12	15.5	$\approx 4log_2 R$

It is assumed that I_o is the supply current of a single gate running at full clock speed, and the supply currents of other gates are scaled by their working frequencies. Therefore, the supply current of each component in multiplex blocks can be expressed in the unit I_o [3], [21], [22]. Table I shows the current breakdown of basic multiplexer blocks. The supply currents of the multiplexers, latches, and clock dividers running at full speed are $1I_o$, $1I_o$, and $2I_o$, respectively. Data in Tables I and II are obtained by manually counting the number of components. In the R:1 electrical funneling E-O interface, the total current consumed by multiplexer blocks is about $5\log_2 R \cdot I_o$. In the R:1 optical weaving E-O interface, all gates share the same current source [3], and the total current is I_o. Assuming that supply voltages are fixed, the power consumptions of each component are proportional to I_o, and all of them can be expressed in the unit P_e, which is the power of a gate.

It is assumed that S_e is the area of a single gate running at full clock speed, and the areas of other gates are scaled by their working frequencies. The area breakdown is similar to the current breakdown [23]. In the R:1 electrical funneling E-O interface, the area for the multiplexer blocks is about $5\log_2 R \cdot S_e$. In the R:1 optical weaving E-O interface,

TABLE III
COMPARISON OF POWER CONSUMPTION P_e AND AREA S_e [UNIT POWER P_e AND UNIT CURRENT S_e ARE DEFINED IN (1)]

Interface	E-O (P_e)	E-O (S_e)	O-E (P_e)	O-E (S_e)
Funneling	$5log_2R$	$5log_2R$	$4log_2R$	$4log_2R$
Weaving	1	$R/2$	3	$R/2+2$

the area for the gates is $(R/2)\cdot S_e$. The power consumption and area of the multiplexer blocks in both R:1 E-O interfaces are summarized in Table III. The data in Table III are obtained by manually counting the number of components. The unit power consumption P_e and unit area S_e are expressed in

$$P_e = I_0(f)\cdot V_{\text{dd}} \qquad S_e = S_0(f). \tag{1}$$

P_e and S_e are both functions of the circuit working frequencies. $I_0(f)$ is assumed to be 0.1–0.5 mA/Gbit/s with 1 V supply voltage (V_{dd}) [14], [24], [25]; $S_0(f)$ is assumed to be 40 μm^2/Gbit/s under 22-nm technology [14]; and f is the data rate of the serial optical signals.

D. Demultiplexer Block

In electrical funneling O-E interfaces, component demultiplexer blocks select one of several output signals and forward the data from the input port to the selected output port. The basic demultiplexer block, which has one input and two outputs, is shown in Fig. 6(b). Three latches are implemented in demultiplexer blocks to store the bits of information [2]. Clock signals are used to select the output signals, and in this design, output 0 is selected at the rising clock edge, and output 1 is selected at the falling clock edge. A 1/2 clock divider is implemented in each stage to provide clock signals with different frequencies. In optical weaving O-E interfaces, phase-shifted clock signals are designed to select one of several outputs directly. There is an array of RZ-to-NRZ converters, which store the bits for the next several cycles. Hence, optical weaving interfaces have the same output waveforms as electrical funneling ones.

Table II shows the current breakdown of basic demultiplexer blocks. The supply current and area of the latches and clock dividers running at full speed are assumed to be the same as those in basic multiplexer blocks. In the 1:R electrical funneling O-E interface, the total current and area consumed by the demultiplexer blocks are about $4\log_2 R \cdot I_o$ and $4\log_2 R \cdot S_e$, respectively. In the 1:R optical weaving O-E interface, there is no demultiplexer implemented because optical signals are deserialized by an array of microresonators directly under the control of the clock signals. The performance of components such as amplifiers and RZ-to-NRZ converters will be analyzed in Section IV-H. The power consumption and area of the demultiplexer blocks in both 1:R O-E interfaces are summarized in Table III.

E. Laser Source

There are N optical wavelengths in both the electrical funneling and optical weaving OI(M, N). Each of them is generated by an independent laser source. The power consumption

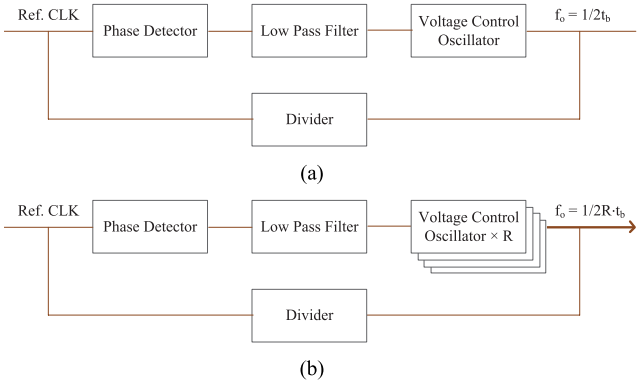

Fig. 7. (a) Clock generator for electrical funneling interfaces has only one VCO. (b) Clock generator for optical weaving interfaces has R cascaded VCOs. Its output frequency is 1/R the frequency of the clock generators for electrical funneling interfaces.

of a single laser P_l is proportional to the receiver sensitivity and inversely proportional to its power conversion efficiency and optical power losses. It is expressed in

$$P_l = \frac{P_s}{L_l \cdot L_c^2 \cdot L_p^d} \cdot \frac{1}{Li^t} = \frac{P_0}{Li^t} \tag{2}$$

where P_s is the receiver sensitivity, which is assumed to be 25 μW (-16 dBm) [26], and L_l is the power conversion efficiency of the laser, which is assumed to be -10 dB [27]. Losses on the optical paths include coupling losses, propagation losses, and modulator insertion losses. L_c is the coupling efficiency between the optical waveguide and the transceiver, which is assumed to be -2 dB [1] for both the transmitter coupler and receiver coupler. L_p is the propagation loss of the optical waveguide in unit length, which is assumed to be -0.12 dB/cm [1], and d is the length of the waveguide. The result of the above four terms is denoted by P_0. The insertion loss L_i is the loss resulting from the insertion of one microresonator along the waveguide. It is assumed to be -0.3 dB [28]–[30], and t is the number of microresonators. Lasers can be classified into two categories: on-chip and off-chip lasers. On-chip lasers are mounted on the die, and the area of each laser S_l is assumed to be 900 μm^2 [27]. On the other hand, lights from off-chip lasers are coupled into the on-chip waveguides via couplers [31].

F. Clock Generator

In electrical funneling and optical weaving E-O interfaces, clock generators are typically implemented by PLLs [2], which multiply a low-frequency reference clock up to high-frequency operating clocks. The PLL circuit for the electrical funneling E-O interface includes a phase detector, low-pass filter, voltage control oscillator (VCO), and divider, as shown in Fig. 7(a). It is able to output high-frequency (1/2t_b in this example) and low-phase-skew clock signals. The reference clock signal and the signal from the VCO are connected to the phase detector, and the output from the phase detector is passed through the low pass filter and then applied to the VCO module. The frequency ratio between the output clocks and the reference clock depends on the division ratio of the divider.

The clock generator for the optical weaving interface is similar to that for the electrical funneling interface, as shown in Fig. 7(b). It includes an R-stage cascaded VCO, where R is the parallel-to-serial ratio [6]. The output frequency of each stage VCO is $1/2Rt_b$. Since the supply current of the VCO is proportional to the output frequency [32], the clock generators for both the electrical funneling and optical weaving interfaces have the same power consumptions. It is assumed that a group of eight E-O interfaces share the same clock generator [2]. The power consumption of the clock generator for each interface P_c is assumed to be 0.5 mW [33]. The area for each interface S_c is assumed to be 180 μm^2/Gbits/s under 22-nm technology [33].

G. Transmitter Module

In electrical funneling and optical weaving E-O interfaces, transmitter modules modulate optical light by microresonators. The overview structure of a transmitter module, which includes a driver and a microresonator, is shown in Fig. 9(a). Output ports of the driver are connected to the p-n junction of the microresonator, which is used as a carrier-injection modulator [19]. When the junction is discharged, the resonance wavelength of the microresonator equals the wavelength of the optical signals, and the output optical signals are minimized. When the junction is charged, the resonance wavelength is shifted away from the wavelength of the optical signals, and the output optical signals are maximized. In optical transmission systems with carrier-injection modulators, the rise time of optical signals is much shorter than the rise time of electrical signals. This is because the relationship between the output optical power and charges in the junction is not linear. The fall time of optical signals is also short because the process to extract carriers out of the junction is very fast [34].

The power consumption of the driver is denoted by P_d. Each time the voltage level of the PN junction is reversed, it is charged or discharged by the driver, where energy is consumed [30]. The power consumption of the microresonator is denoted by P_m. When the voltage level of the PN junction is high, it is forward biased, and energy is consumed because of the direct current flowing through the p-n junction. Power consumptions P_d and P_m are expressed in

$$P_d = f \cdot C_m \cdot V_m^2 \qquad P_m = I_m \cdot V_m. \tag{3}$$

P_d is a function of the data rate f [30]; C_m is the input capacitance of the microresonator, which is assumed to be 30 fF [34]; and V_m is the supply voltage of the microresonator, which is assumed to be 2 V [34]. P_m, on the other hand, is not a function of the data rate f, and I_m is the direct current of the microresonator, which is assumed to be 60 μA [34]. The area of each transmitter module S_m is related to the size of the microresonator, which is assumed to be 125 μm^2 [7].

It is assumed that bits 0 and 1 are evenly distributed in the input sequences. An example of the output waveform of drivers in electrical funneling interfaces is shown in Fig. 8(a). Each time a bit is transmitted, there is a 1/4 chance that the voltage level of the driver output changes from low to high, and the p-n junction of the microresonator is charged.

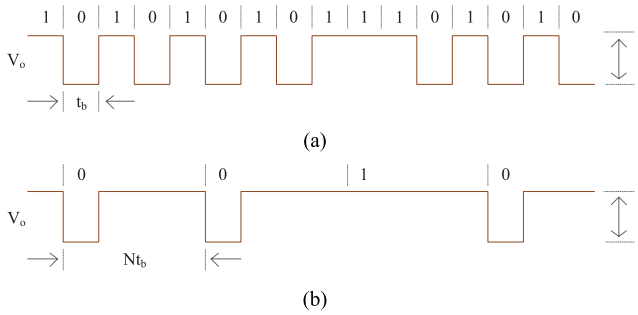

Fig. 8. (a) Example of the output waveform of drivers in electrical funneling interfaces. (b) Example of the output waveform of drivers in optical weaving interfaces. Its duty cycle is $1/R$.

TABLE IV
POWER CONSUMPTION OF DRIVER P_d AND MICRORESONATOR P_m [POWER P_d AND POWER P_m ARE DEFINED IN (3)]

Interface	E-O (P_d)	E-O (P_m)	O-E (P_d)	O-E (P_m)
Funneling	$1/4$	$1/2$	0	0
Weaving	$1/2$	R	1	R

On the other hand, there is a 1/2 chance that the voltage level of the driver output is high, and energy is consumed by the direct current flowing through the junction. The power consumption of driver and microresonator is $1/4P_d$ and $1/2P_m$, respectively. An example of the output waveform of drivers in optical weaving interfaces is shown in Fig. 8(b). Totally, there are R pairs of drivers and microresonators. The duty cycle of each output waveform is $1/R$, and the power consumption of each driver and each microresonator is $1/(2R) \cdot P_d$ and P_m. The total power consumption in E-O interfaces is summarized in Table IV, where data are obtained by manually counting the number of components. In addition, for each microresonator in the transmitter module, the tuning power consumption is denoted by P_t, which is assumed to be 0.05 mW [29], [35].

H. Receiver Module

In electrical funneling and optical weaving O-E interfaces, the receiver modules filter optical light by microresonator, and then convert optical signals into electrical signals. The overview structure of a transmitter module, which includes a driver, a microresonator, a photodetector, an amplifier, and a converter, is shown in Fig. 9(b). In electrical funneling interfaces, the passive microresonators do not consume energy because their resonance wavelengths are fixed. In optical weaving interfaces, each microresonator is forward biased by a driver. For every $4t_b$ time, the voltage level of the driver output is low for t_b time, and the resonance wavelength of the microresonator shifts back to the wavelength of light. At that time, optical light is filtered into the corresponding photodetector.

Optical signals are first converted into RZ-coded electrical signals by the photodetector and amplifier. They are then converted into NRZ-coded signals by RZ-to-NRZ converters [36]. Totally, there are R pairs of amplifiers and converters. The power consumptions of each amplifier and each converter

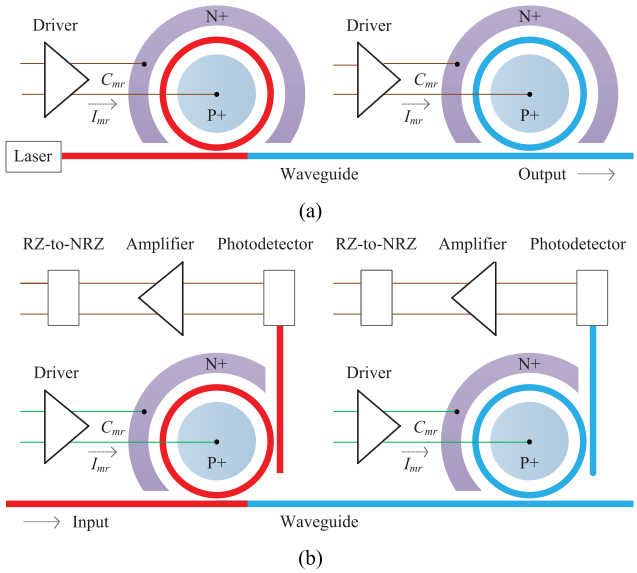

Fig. 9. (a) In E-O interfaces, the transmitter modules include drivers and microresonators. (b) In O-E interfaces, the receiver modules include drivers, microresonators, photodetectors, amplifiers, and NZ-to-NRZ converters. The red lines stand for optical signals in waveguide.

are $1/R \cdot P_e$ and $2/R \cdot P_e$. The area of each amplifier and each converter is $1/2S_e$ and $2/R \cdot S_e$. These are summarized in Table III. In addition, in optical weaving O-E interface, the power consumptions of each driver and each microresonator are $1/R \cdot P_d$ and P_m, respectively. The total power consumptions in O-E interfaces are summarized in Table IV. The tuning power for each microresonator in the receiver module is P_t.

V. Quantitative Analysis and Comparison

In this section, the performances of electrical funneling interfaces and optical weaving interfaces are quantitatively analyzed and compared in terms of energy consumption, area, and latency. In addition, inter/intra-chip interconnects using electrical funneling interfaces and optical weaving interfaces are also analyzed and compared.

A. Analytical Models and Assumptions

This paper provides analytical models on energy consumptions, areas, and latencies for both electrical funneling and optical weaving interfaces. Although the values of parameters depend on the specific implementations and technologies, the analytical models are general to different technologies. Some of the parameters may change because of the advancement of technologies. In case studies, all the parameters are assumed based on state-of-the-art technologies. In particular, some parameters have large variations if different technologies are applied, such as the unit supply current I_0 and the unit area S_e of electrical circuits, which are defined in Section IV. For those parameters, we make multiple assumptions and calculate a group of results on based on those assumptions.

B. Energy Consumption

Energy consumption is the physical layer energy required to move data per bit, which is proportional to the power consumption of the transmission system and inversely proportional to the total data rate of the interconnects. It is assumed that the data rate of the optical wavelength is f, and the parallel-to-serial ratio is R, which equals M/N in OI(M, N). The power consumptions of the electrical funneling E-O interface and electrical funneling O-E interface are denoted by P_{feo} and P_{foe}, which are expressed in

$$P_{\text{feo}} = 5\log_2 RP_e + P_c + \frac{1}{4}P_d + \frac{1}{2}P_m + P_t + \frac{P_o}{L_i} \quad (4)$$

$$P_{\text{foe}} = 4\log_2 RP_e + P_t + \left(\frac{1}{L_i} - 1\right)P_o \quad (5)$$

where P_e, P_c, P_d, P_m, P_t, and P_o are the power consumptions of the gate, clock generator, driver, microresonator, tuner, and laser, respectively. The values of P_e, P_d, and P_m are summarized in Tables III and IV. In the E-O interface, there is one clock generator whose power consumption is P_c. One microresonator is implemented along the waveguide so that the power consumption of the tuner is P_t, and the power consumption of the laser is P_o/L_i, where L_i is the power loss of each microresonator. In the O-E interface, there is one microresonator implemented so that the power consumption of the tuner is P_t. The microresonator will increase the power consumption of the laser source, and the increment is $(1/L_i - 1)P_o$. The power consumptions of optical weaving E-O interface and optical weaving O-E interface are denoted by P_{weo} and P_{woe}, which are expressed in

$$P_{\text{weo}} = P_e + P_c + \frac{1}{2}P_d + RP_m + RP_t + \frac{P_o}{L_i^R} \quad (6)$$

$$P_{\text{woe}} = 3P_e + P_d + RP_m + RP_t + \left(\frac{1}{L_i^R} - 1\right)P_o \quad (7)$$

where the values of P_e, P_d, and P_m are summarized in Tables III and IV. There is one clock generator in the E-O interface with power consumption P_c. R microresonators are implemented along the waveguide in both the E-O interface and O-E interface. Assuming the E-O and O-E interfaces are independently analyzed, the power consumptions of the lasers in these two interfaces are P_o/L_i^R and $(1/L_i^R - 1)P_o$, respectively, and the power consumptions of the tuners are both RP_t. Energy consumption can be expressed as P/f, where P is the power consumption and f is the data rate.

The energy consumptions of 4:1, 8:1, and 16:1 electrical funneling and optical weaving E-O interfaces versus the data rate of an optical interconnect are plotted in Fig. 10, while the energy consumptions of 1:4, 1:8, and 1:16 electrical funneling and optical weaving O-E interfaces versus the data rate of an optical interconnect are plotted in Fig. 11. The data are obtained from analytical models. The length of the optical waveguide is assumed to be 50 cm, the unit supply current of the gates and latches I_0 is assumed to be 0.1–0.5 mA/Gbit/s with 1 V supply voltage [14], [24], [25], and the data rate of the serial optical interconnect ranges from 2 to 30 Gbits/s. The data rate of each parallel electrical interconnect is equal to the data rate of the serial optical interconnect divided by R. The energy consumptions can be scaled to other technologies by scaling the unit current I_0.

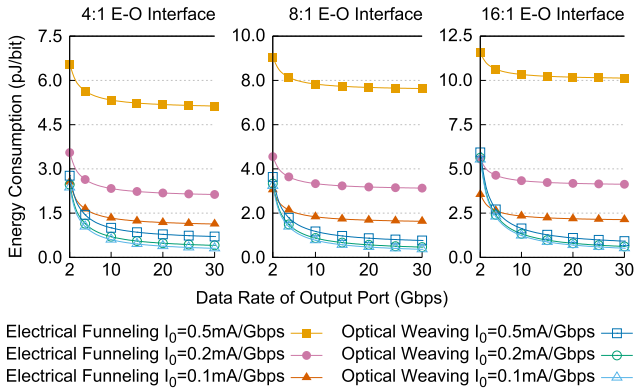

Fig. 10. Energy consumptions of 4:1/8:1/16:1 electrical funneling and optical weaving E-O interfaces versus the data rate of serial optical interconnect. It is assumed that the unit current of electrical circuits equals 0.5/0.2/0.1 mA/Gbit/s. Data are obtained from analytical models.

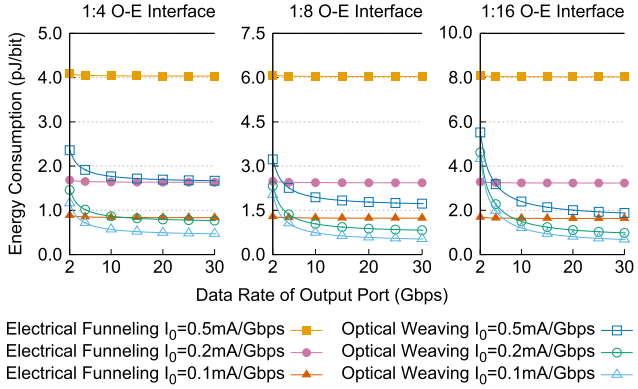

Fig. 11. Energy consumptions of 1:4/1:8/1:16 electrical funneling and optical weaving O-E interfaces versus the data rate of serial optical interconnect. It is assumed that the unit current of electrical circuits equals 0.5/0.2/0.1 mA/Gbit/s. Data are obtained from analytical models.

When the unit current I_0 is 0.2 mA/Gbit/s, and the data rate f increases, the energy consumption improvement of the 8:1 optical weaving E-O interface over the electrical funneling interface increases from 26.7% to 85.1%, where the energy consumption improvement of the 1:8 optical weaving O-E interface over the electrical funneling interface increases from 6.4% to 66.0%. Compared with electrical funneling interfaces, optical weaving interfaces have fewer gates and latches, whose power consumptions are proportional to the date rate. On the other hand, they have more microresonators and lasers, whose power consumptions are not related to the data rate. Therefore, when the date rate is increased, the difference in energy consumption between the two types of interfaces increases. It is also showing that when the parallel-to-serial ratio R is increased, the energy consumptions of the electrical funneling and optical weaving interfaces both increase because of the increment of the gate and latch count.

C. Area

The areas of interfaces consist of two parts: areas of electrical components, such as gates and clock generators, and areas of optical components, such as microresonators and on-chip lasers. It is assumed that the data rate of the optical wavelength is f, and the parallel-to-serial ratio is R, which

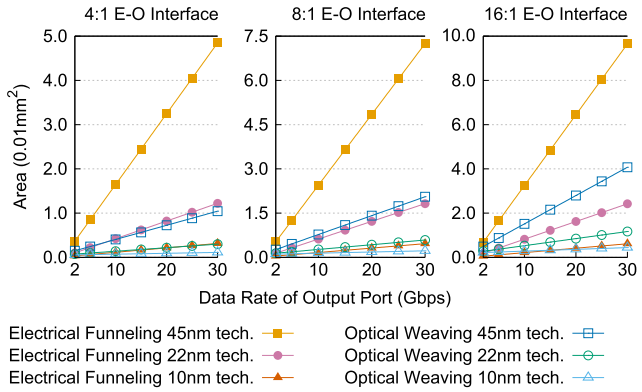

Fig. 12. Areas of 4:1/8:1/16:1 electrical funneling and optical weaving E-O interfaces versus the data rate of serial optical interconnect. It is assumed that the technology node is 45/22/10 nm. Data are obtained from analytical models.

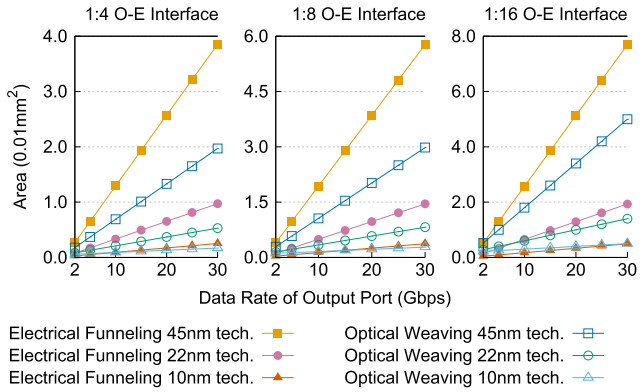

Fig. 13. Areas of 1:4/1:8/1:16 electrical funneling and optical weaving O-E interfaces versus the data rate of serial optical interconnect. It is assumed that the technology node is 45/22/10 nm. Data are obtained from analytical models.

equals M/N in OI(M, N). The areas of the electrical funneling E-O interface and electrical funneling O-E interface are denoted by S_{feo} and S_{foe}, which are expressed

$$S_{\text{feo}} = 5\log_2 RS_e + S_c + S_m + S_l \tag{8}$$

$$S_{\text{foe}} = 4\log_2 RS_e + S_m \tag{9}$$

where S_e, S_c, S_m, and S_l are the areas of the gate, clock generator, microresonator, and laser, respectively. The values of S_e are summarized in Table III. In the E-O interface, there is one clock generator whose area is S_c and one laser source whose area is S_l. The areas of the periphery circuits for the microresonator are all included in S_m. A microresonator is implemented along the waveguide in both the E-O interface and O-E interface, and the areas of the microresonators in these two interfaces are S_m. The areas of optical weaving E-O interface and optical weaving O-E interface are denoted by S_{weo} and S_{woe}, which are expressed in

$$S_{\text{weo}} = \frac{M}{2N}S_e + S_c + \frac{M}{N}S_m + S_l \tag{10}$$

$$S_{\text{woe}} = \left(\frac{M}{2N} + 2\right)S_e + \frac{M}{N}S_m \tag{11}$$

where the values of S_e are summarized in Table III. In the E-O interface, there is one clock generator whose area is S_c and R laser sources, whose areas are RS_l. R microresonators are implemented along the waveguide in both the E-O interface and O-E interface. The areas of the microresonators in these two interfaces are RS_m.

The areas of 4:1, 8:1, and 16:1 electrical funneling and optical weaving E-O interfaces versus the data rate of an optical interconnect are plotted in Fig. 12, while the areas of 1:4, 1:8, and 1:16 electrical funneling and optical weaving O-E interfaces versus the data rate of an optical interconnect are plotted in Fig. 13. The data are obtained from analytical models. The technology node is assumed to be 45, 22, and 10 nm. The unit area of gates and latches S_e is assumed to be 160 μm^2/Gbits/s under 45-nm technology, 40 μm^2/Gbits/s under 22-nm technology, and 10 μm^2/Gbits/s under 10-nm technology [14], and the data rate of the serial optical interconnect ranges from 2 to 30 Gbits/s. The data rate of each parallel electrical interconnect equals to the data rate of the serial optical interconnect divided by R. The area can be scaled to other technologies by scaling the unit area S_e.

When the unit area S_e is 40 μm^2/Gbits/s, and the data rate f increases, the area improvement of the 8:1 optical weaving E-O interface over the electrical funneling interface increases from 0.4% to 67.7%, while the area improvement of the 1:8 optical weaving O-E interface over the electrical funneling interface increases from -36.4% to 43.5%. Similar to energy consumption, the area of gates and latches is assumed to be proportional to the data rate, and the area of microresonators and lasers is not related to the data rate. When the date rate is increased, the difference in area between the two types of interfaces increases. It is also showing that when the parallel-to-serial ratio R is increased, the area of the two types of interfaces also increases.

D. Latency

The latency of interchip interconnects is the amount of time it takes for the head of signals to travel from end to end, and it includes three parts: 1) the multiplexer/demultiplexer delay; 2) the RC delay; and 3) the propagation delay. It is assumed that the bit time of the serial optical signals is t_b and the propagation delay is t_p. The latencies of electrical funneling and optical weaving E-O interfaces are denoted by T_{feo} and T_{weo}, and these are expressed in (12), while the latencies of O-E interfaces are denoted by T_{foe} and T_{woe}, and these are expressed in (13). The multiplexer delays in the electrical funneling and optical weaving E-O interfaces are $(R-1)\cdot t_b$ and 0, respectively, the average demultiplexer delays in the electrical funneling and optical weaving O-E interfaces are $(R-1)\cdot t_b$ and $(R/2-1/2)\cdot t_b$, respectively, and the RC delays in all interfaces are assumed to be t_b. The propagation delay of the interconnect is denoted by t_p

$$T_{\text{feo}} = Rt_b + t_p \quad T_{\text{weo}} = t_b + t_p \tag{12}$$

$$T_{\text{foe}} = Rt_b + t_p \quad T_{\text{woe}} = \frac{R+1}{2}t_b + t_p. \tag{13}$$

The total latency is the summation of the multiplexer/demultiplexer delay, RC delay, and propagation delay. t_b is expressed as $1/f$, where f is the data rate of the serial optical signals. t_p is expressed as nL/c [37], where n is the refractive index of the optical interconnect, which is assumed to be 1.47 [38]. c is the light speed in a vacuum, which is 30 cm/ns, and L is the length of the optical waveguide.

E. Optical Weaving Versus Electrical Funneling

The performance of the electrical funneling OI(M, N) and optical weaving OI(M, N) varies based on different combinations of M and N. There are N pairs of E-O and O-E interfaces with N optical wavelengths in OI(M, N). Assuming that the total data rate of OI(M, N) is f, the load of the data transmission is equally distributed among the N wavelengths. The data rate on each pair of interfaces is f/N. The power consumptions of the electrical funneling OI(M, N) and optical weaving OI(M, N) are denoted by P_f and P_w, which are expressed in

$$P_f = 9\log_2\frac{M}{N}P_e + P_c + \frac{P_d}{4} + \frac{N}{2}P_m + 2NP_t + \frac{NP_o}{L_i^{2N}} \tag{14}$$

$$P_w = 4P_e + P_c + \frac{3P_d}{2} + 2MP_m + 2MP_t + \frac{NP_o}{L_i^{2M}} \tag{15}$$

where P_e, P_c, P_d, P_m, P_t, and P_o are the power consumptions of the gate, clock generator, driver, microresonator, tuner, and laser, respectively. It is assumed that the power consumptions of the gate, clock generator, and driver are proportional to the data rate. Therefore, their power consumptions are $1/N\cdot 0P_e$, $1/N\cdot P_c$, and $1/N\cdot P_d$ under data rate f/N. On the other hand, power consumptions of the microresonator and tuner are unaffected by the data rate, and their power consumptions are still P_m and P_t. The total power consumption of OI(M, N) equals the power consumption of each pair of interfaces multiplied by N. The laser power is related to the number of microresonators that optical light will pass by. In the electrical funneling OI(M, N), there are $2N$ microresonators: N in the E-O interface and N in the O-E interface. In the optical weaving OI(M, N), there are $2M$ microresonators in total: M in the E-O interface and M in the O-E interface. The areas of electrical funneling OI(M, N) and optical weaving OI(M, N) are denoted by S_f and S_w, which are expressed in

$$S_f = 9\log_2\frac{M}{N}S_e + S_c + 2NS_m + NS_l \tag{16}$$

$$S_w = \left(\frac{M}{N} + 2\right)S_e + S_c + 2MS_m + NS_l \tag{17}$$

where S_e, S_c, S_m, and S_l are the areas of the gate, clock generator, microresonator, and laser, respectively. It is also assumed that the areas of the gate and clock generator are proportional to the data rate. Therefore, their areas are $1/N\cdot S_e$ and $1/N\cdot S_c$ under data rate f/N. The values of these areas can be scaled based on the corresponding CMOS technology. On the other hand, the areas of the microresonator and laser are unaffected by the data rate, and their areas are still P_m and S_l. The numbers of microresonators in the electrical funneling

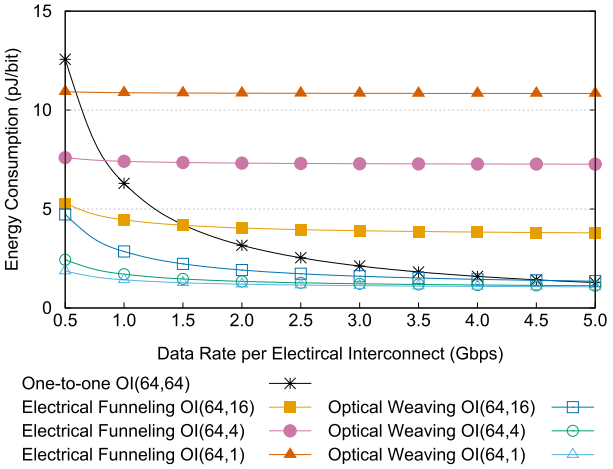

Fig. 14. Energy consumptions of electrical funneling OI(64, N) and optical weaving OI(64, N) versus the data rate per electrical interconnect. There are 64 parallel electrical interconnects and 64/16/4/1 optical wavelengths. Unit current $I_o = 0.2$ mA/Gbit/s. The length of the optical waveguide is 50 cm. Data are obtained from analytical models.

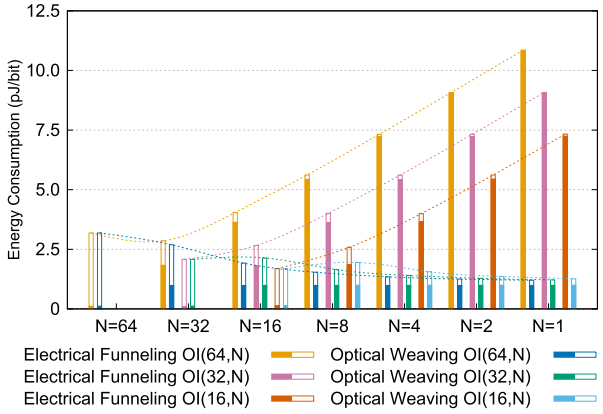

Fig. 16. Comparison of energy consumptions of electrical funneling OI(M, N) and optical weaving OI(M, N). There are 64/32/16 parallel electrical interconnects and 1–64 optical wavelengths. Unit current $I_o = 0.2$ mA/Gbit/s. Solid bars stand for energy electrical modules, and empty bars stand for optical modules. The length of the optical waveguide is 50 cm. The data rate per electrical interconnect is 2 Gbits/s. Data are obtained from analytical models.

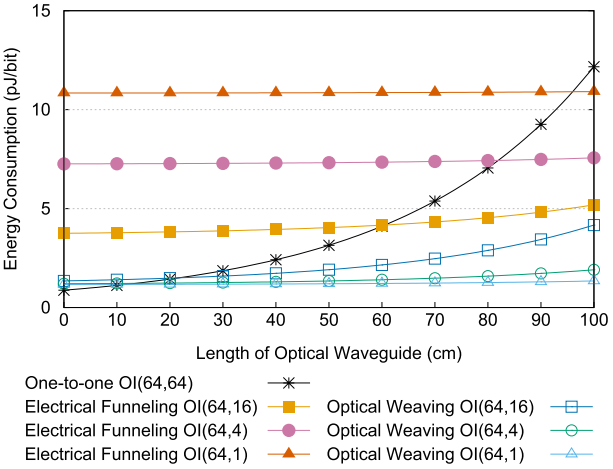

Fig. 15. Energy consumptions of electrical funneling OI(64, N) and optical weaving OI(64, N) versus the length of optical waveguide. There are 64 parallel electrical interconnects and 64/16/4/1 optical wavelengths. Unit current $I_o = 0.2$ mA/Gbit/s. The data rate per electrical interconnect is 2 Gbits/s. Data are obtained from analytical models.

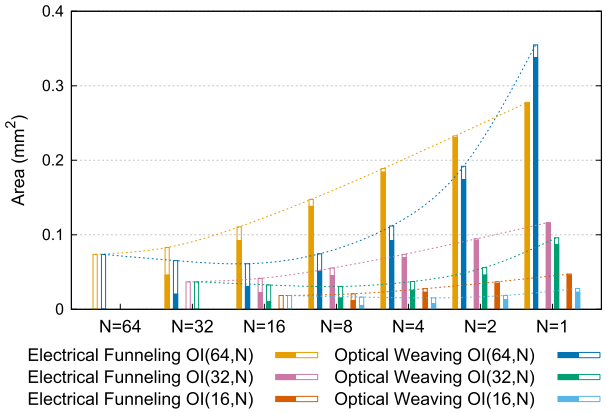

Fig. 17. Comparison of areas of electrical funneling OI(M, N) and optical weaving OI(M, N). There are 64/32/16 parallel electrical interconnects and 1–64 optical wavelengths. The technology node is assumed to be 22 nm. Solid bars stand for energy electrical modules, and empty bars stand for optical modules. The length of the optical waveguide is 50 cm. The data rate per electrical interconnect is 2 Gbits/s. Data are obtained from analytical models.

OI($M.N$) and optical weaving OI($M.N$) are $2N$ and $2M$, respectively. It is assumed that the laser sources are implemented on the die. There are N lasers in total.

It is assumed that the unit supply current of gate I_o equals 0.2 mA/Gbit/s. Assuming the length of the optical waveguide is 50 cm, the energy consumptions of the electrical funneling OI(64, N) and optical weaving OI(64, N) versus the data rate per electrical interconnect are plotted in Fig. 14. Assuming that the data rate of each electrical interconnect is 2 Gbits/s, the energy consumptions of the electrical funneling OI(64, N) and optical weaving OI(64, N) versus the length of optical waveguide are plotted in Fig. 15. The data are obtained from analytical models. There are 64 parallel electrical interconnects, and the number of optical wavelengths N is 1, 4, 16, and 64. If N equals 64, one electrical interconnect is directly mapped to one optical wavelength, and SerDes are not necessary in OI(M, N). This configuration is referred to as one-to-one mapping in the analysis. If N equals 1, there is only one pair of E-O and O-E interfaces, and the parallel-to-serial ratio is maximized.

When the data rate of each electrical interconnect increases from 0.5 to 5 Gbits/s, the energy consumption improvement of the optical weaving OI(64, 4) over the electrical funneling OI(64, 4) increases from 67.9% to 84.5%, and when the length of the optical interconnect increases from 0 to 100 cm, the energy consumption improvement decreases from 83.4% to 74.8%. This is because the optical weaving OI(64, 4) has more microresonators and lasers than the electrical funneling OI(64, 4). Hence, its energy consumption is more related to the energy consumptions of the optical components. When the data rate is increased, more bits can be transmitted with the lasers and microresonators consuming the same amount of energy. On the other hand, when the length of

the optical waveguide is increased, the attenuation is increased. Therefore, more energy will be consumed by the laser sources. The analysis also shows that when the parallel-to-serial ratio is increased, the energy consumption of electrical funneling interfaces will increase, while, on the other hand, that of optical weaving interfaces will decrease.

Assuming that the unit supply current of gate I_o is 0.2 mA/Gbits/s, the energy consumptions of the electrical funneling OI(M, N) and optical weaving OI(M, N) under different combinations of M and N are plotted in Fig. 16. Assuming the technology node is 22 nm, the areas of the electrical funneling OI(M, N) and optical weaving OI(M, N) are plotted in Fig. 17. The data are obtained from analytical models. It is assumed that there are 64, 32, or 16 parallel electrical interconnects, and the number of optical wavelengths N is 1–64. The length of optical interconnect is 50 cm, and the data rate of each electrical interconnect is fixed at 2 Gbits/s. In Figs. 16 and 17, energy consumptions and areas consist of two parts. The solid bars represent the energy consumption and area, respectively, of electrical components, including gates, clock generators, drivers, and tuners, while the empty bars stand for those of optical components, including microresonators and lasers.

When N decreases from 32 to 1, the energy consumption improvement of the optical weaving OI(64, N) over the electrical funneling OI(64, N) increases from 5.7% to 88.9%. The area improvement increases from 21.2% to 49.5%, and then decreases to -27.8%. This is because when the parallel-to-serial ratio is increased, the working frequencies of the interfaces increase linearly. In electrical funneling interfaces, the number of gates and latches is increased so that the supply current and area of each interface increase superlinearly. In optical weaving interfaces, the number of gates is fixed, but the number of transistors in each gate is increased. Hence, the supply current of each interface increases linearly, and the area increases superlinearly. The energy consumption of the electrical components in the electrical funneling OI(64, N) is increased, while that in the optical weaving OI(64, N) remains unchanged. Besides this, when N decreases, the energy consumptions and areas of the optical components will decrease because the total number of laser sources is decreased.

VI. Conclusion

In this paper, a method is proposed to model two types of E-O and O-E interfaces for inter/intra-chip interconnects in terms of energy consumption, area, and latency: traditional electrical funneling interfaces, which serialize/deserialize signals by SerDes, and optical weaving interfaces, which serialize/deserialize signals by TDM optical systems. Our analysis shows that optical weaving interfaces enjoy lower energy consumption, smaller area, and lower latency than electrical funneling interfaces. In particular, if the parallel-to-serial ratio of the interfaces is increased from 1 to 64, the energy spent per bit on electrical funneling interfaces is increased by 241%, while the energy spent per bit on optical weaving interfaces is decreased by 62.3%. In addition to energy consumption, the analysis also shows that the area and latency of optical weaving interfaces are smaller than those of electrical funneling interfaces. Finally, we integrate the analysis models for SerDes in tool OEIL [39].

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