3D Optical Networks-on-chip (NoC) for Multiprocessor Systems-on-chip (MPSoC)

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***Abstract*— Networks-on-chip (NoC) is emerging as a key on-chip communication architecture for multiprocessor systems-on-chip (MPSoC). In traditional electronic NoCs, high bandwidth can be obtained by increasing the number of parallel metallic wires at the cost of more energy consumption. Optical NoCs are thus proposed to achieve low-power ultra-high-bandwidth data transmission in optical domain. Electronic control technology could be a complement to the optical networks. Besides NoCs, three-dimensional integrated circuits (3D ICs) are another attractive solution for system performance improvement by reducing the interconnect length. The investigation of using 3D IC as a platform for the realization of mixed-technology electronic-controlled optical NoC has not been addressed until recently. In this paper, we propose a 3D electronic-controlled optical NoC implemented in a TSV-based (through-silicon via) two-layer 3D chip. The upper device layer is an optical layer. It integrates an optical data transmission network, which is responsible for optical payload packets transmission. The bottom device layer is an electronic layer. It contains an electronic control network, which is used to route control packets and configure the optical network. We built an 8x8 mesh-based 3D optical NoC, with a 45nm electronic control network. Power comparison with a matched 2D electronic NoC shows that the optical NoC can reduce power consumption significantly. For 2048B packets, it has a 70% power reduction. End-to-end delay (ETE delay) and network throughput of the two NoCs under varying injection rates were evaluated for comparison. The results show that ETE delay of the optical NoC is much smaller than the electronic NoC when the network becomes congested. Take 4096B packets for example, it is $18.7\mu s$ in the optical NoC with an injection rate of 0.5, while $33.5\mu s$ in the electronic one. A maximum throughput of $478Gbps$ can be offered by the optical NoC using 32Gbps optical link bandwidth. Because of the low resource utilization of circuit switching, the maximum throughput of the optical NoC is slightly lower than the electronic one.**[1]

I. Introduction

With the increasing complexity of multiprocessor systems-on-chip (MPSoC), global communication on chip has become a major challenge for system performance improvement within restricted power and area budgets [1]. Networks-on-chip (NoCs) are emerging as an alternative to existing dedicated interconnection and shared bus [2] [3]. It relieves on-chip communication issues by improving the bandwidth, power efficiency and scalability [4].

However, due to the limited bandwidth and high power dissipation of metallic interconnects, conventional electronic NoC may not satisfy the future performance and power requirement [5] [6]. Optical NoC is a new approach promising to empower an enormous bandwidth increase with much less power consumption [7]. It is based on optical interconnects and optical on-chip routers [8] [9]. Such optical solutions are made possible by recent developments in nanoscale silicon photonics and integrated optical devices [10] [11]. Because of the difficulty in photonic processing and buffering, optical on-chip router proposed in literature usually employs a hybrid design, using electrical signals to control the optical switching fabrics. A. Shacham et al. have proposed a photonic NoC with hybrid architecture in [9], where an optical network is overlapped with an electronic control network. The optical network is used for high-speed optical data transmission, while the electronic control network is for distributed control and short message exchanges.

Optical on-chip routers are the most important components of the optical NoCs. Several optical routers with traditional crossbar architecture or optimized architectures have been proposed in literature. A silicon microring resonator-based switch node was proposed for photonic mesh NoCs in [12]. It is a full-connected crossbar architecture comprising of silicon microresonator arrays. A NxN λ-router with high scalability was proposed in [13], based on WDM technology and passive switching. Cygnus is a non-blocking optical router proposed in [14]. Compared with other optical routers, it has fewer microresonators, less power consumption and less optical power insertion loss. ODOR was proposed in [15] especially for optical NoCs using XY routing algorithm.

In addition to NoC architecture, three-dimensional integrated circuit (3D IC) offers an attractive solution for overcoming the barriers to interconnect scaling, thereby offering an opportunity to continue performance improvements using CMOS technology, with smaller form factor, higher integration density, and the support for the realization of mixed-technology chips. Among several 3D integration technologies, through-silicon via (TSV) approach is the most promising one and therefore is the focus of the majority of 3D integration R&D activities [16]. In a TSV-based 3D chip, multiple device layers are stacked together with direct vertical interconnects tunneling (also called through-silicon via)through them.

To combine the benefits of NoCs and 3D ICs, 3D NoCs have been proposed in [17] to offer better performance, especially for 3D network topologies. B. S. Feero et al.

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demonstrated that the 3D realization of both mesh and tree-based NoCs could improve the performance significantly by reducing the interconnects length. Due to the manufacturing challenges, multiple-layer 3D NoCs may be not practical at this moment. But the two-layer 3D realization has already improved the performance greatly.

The investigation of using multiple-layer 3D ICs as a platform for the realization of mixed-technology electronic-controlled optical NoC has not been addressed until recently. In this paper, we propose a 3D electronic-controlled optical NoC for MPSoC, using Cygnus optical routers. It is implemented in a TSV-based two-layer 3D chip. The upper device layer is an optical layer. It integrates an optical data transmission network, which is responsible for high-speed optical payload transmission. The bottom device layer is an electronic layer. It contains an electronic control network, which is used to route control packets and configure the optical network. The two device layers are stacked together with TSVs. We simulated an 8x8 mesh-based 3D optical NoC with a 45nm electronic control network, and compared it with a 45nm 8x8 mesh 2D electronic NoC. Through detailed simulation-based analysis of the power consumption and network performance, we can demonstrate that the optical NoC proposed in this paper could empower high throughput of data transmission with dramatic power reduction.

The paper is organized as follows: Section II introduces the Cygnus optical router used in our 3D optical NoC. Section III talks about the network topology, routing algorithm, and the protocol. Section IV details the simulations of the 3D optical NoC and a referenced 2D electronic NoC, as well as the comparisons between them in power and performance aspects. Section V draws a conclusion of this paper.

II. Router

Optical NoCs are based on optical on-chip routers and optical interconnects. Optical routers are important components which implement the routing and flow control functions. In this paper, we use a novel optical router called Cygnus (Fig. 1) proposed in [14]. Cygnus is a strictly non-blocking optical 5x5 router for mesh or torus optical NoCs. It has five bidirectional ports, including the injection/ejection, north, south, west and east ports. Each injection/ejection port can connect a functional core through EO/OE interfaces. The functional core could be a processor, a memory controller, or a peripheral device, etc. Cygnus consists of an optical switching fabric and an electronic control unit. The electronic control unit is responsible for configuring the optical switching fabric by electrical signals. The optical switching fabric is used to switch light signals from an input port to an output port according to the configuration.

A. Optical Switching Fabric

The optical switching fabric implements a 5x5 switching function for the five bidirectional ports. It is built from two basic 1x2 switching elements(Fig. 2), including the parallel switching element and the crossing switching element. Both of the two switching elements consist of one microresonator

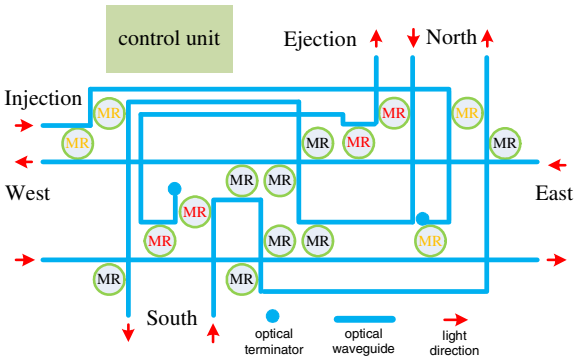

Fig. 1. Layout of Cygnus Router

and two waveguides. The microresonator has an on-state resonance wavelength λ_{on}. When the microresonator is powered on, light signals with wavelength λ_{on} will be coupled into the microresonator and directed to the drop port. On the other hand, when the microresonator is powered off, light signals with wavelength λ_{on} will propagate from the input port to the through port. The 5x5 switching function could be implemented by configuring the microresonators accordingly in the optical switching fabric.

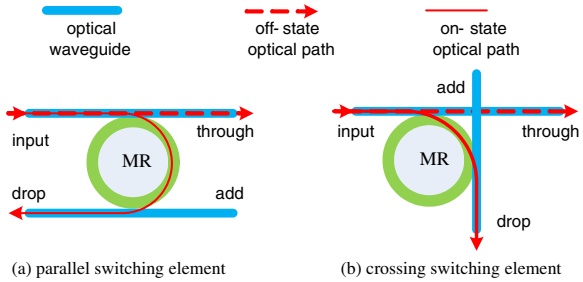

Fig. 2. Two basic 1x2 switching elements

The internal structure of the Cygnus switching fabric has been optimized to minimize waveguide crossings and power consumption. It takes advantage of passive routing to minimize the microresonators power consumption. No microresonator will be in the on-state if light travels between the east and west or between the south and north. And only one microresonator will be powered on if the light has to make a turn or use the injection/ejection port. Such passive routing feature guarantees that the maximum power consumption for dimension order routing is a small constant, regardless of the network size [14].

B. Electronic Control Unit

The electronic control unit is built from traditional CMOS transistors. It uses electrical signals to configure the optical switching fabric by powering on or off microresonators. Each control unit also has five bidirectional ports as the optical switching fabric. A functional core can be connected to the injection/ejection port of the electronic control unit.

III. NETWORK

In our 3D optical NoC, there are two logically overlapped networks, including an optical data transmission network and an electronic control network. The former is a network of Cygnus optical switching fabrics, interconnected by optical interconnects. The latter is another network of Cygnus electronic control units, interconnected by metallic interconnects. We separate the two networks physically by implementing them in two device layers of a 3D chip, which are stacked together with TSVs. In addition, control information and payload are separated into control packets and payload packets. Control packets are routed in the electronic network and payload packets are transmitted in the optical network.

A. Topology

Topology determines how the nodes in the network are connected with each other. In a multiple-hop topology, packets may travel one or more intermediate nodes before arriving at the target node [18]. Regular multiple-hop topologies such as mesh and torus are widely used in NoCs. We can use different topologies for the optical data transmission network and the electronic control network respectively. In this paper, we use mesh topology for both of them.

Fig. 3 shows the architecture of a 4x4 mesh-based 3D optical NoC. It is implemented in a TSV-based two-layer 3D chip in a three-dimensional environment. The optical layer integrates an optical data transmission network, which connects the optical switching fabrics of all the Cygnus routers using optical interconnects. The electronic layer contains a network of Cygnus electronic control units and functional cores. Each functional core is attached to a local electronic control unit. Functional cores are also connected with the corresponding optical switching fabrics through EO/OE interfaces. We use 1-bit wide bidirectional optical interconnects for the optical data transmission network, and 32-bit wide bidirectional metallic interconnects for the electronic control network.

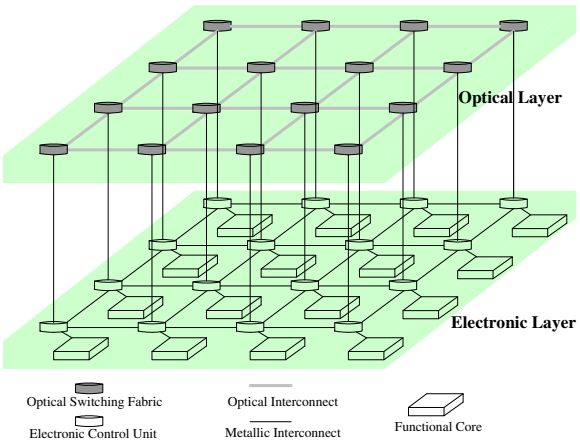

Fig. 3. 4x4 mesh-based 3D optical NoC architecture

B. Routing Algorithm

Routing determines the path selected to route packets from source to destination. Efficient routing is critical to the whole performance. Deterministic routing algorithm always establishes the same path between every pair of nodes, where the path is a function of the source and target addresses. Dimension-order routing is a popular deterministic algorithm because of its simplicity, especially for mesh and torus. XY routing (2D dimension-order routing) is deadlock-free for mesh. In this paper, we use XY routing algorithm for control packets.

C. Protocol

Circuit switching involves a physical path from source to destination which is reserved prior to data transmission. In packet switching, however, packets containing routing information are forwarded on a per-hop basis [19]. In our 3D optical NoC, circuit switching is adopted, in which an optical path is reserved before payload transmission. There are two kinds of control packets, including the setup packet for optical path setup and the tail packet for path release. Control packets only contain necessary routing information, such as the source and target addresses. They are routed in the electronic control network in a manner of packet switching. After path setup, payload packets are transmitted along the reserved optical path in a high speed without buffering.

More specifically, when a functional core wants to communicate with another one, it first sends a setup packet to its local electronic control unit. The setup packet is forwarded in the electronic control network according to routing algorithm. Optical switching fabrics in the routing path are then configured by the corresponding electronic control units. For example, if the current electronic control unit chooses west output port for the setup packet, it will also reserve the west output port of the corresponding optical switching fabric by powering on microresonators accordingly. If the setup packet arrives at the destination, an acknowledge bit will be sent back along the optical path. If the source receives the acknowledge bit, it will send payload data along the reserved optical path. A tail packet would be sent out with the last flit of the payload packet. It travels along the routing path and tears down the optical path by configuring related optical switching fabrics.

D. Physical Design

The electronic control network of an 8x8 mesh-based 3D optical NoC was synthesized using Synopsys Design Compiler, based on the STMicroelectronics 45nm CMOS library. Synthesized netlist was placed and routed using Cadence Encounter v7.1, employing seven metal layers. In the physical implementation stage, we used a divide and conquer strategy to implement the physical designs of the electronic control network. In this approach, the whole design was partitioned into modules. Each of them was carefully optimized to minimize the area and power dissipation while TSVs were retained as internal pins. These modules were hardened into

high-speed macros as black boxes on which we specified the timing and power constraints for global on-chip network connection optimizations. We also generated a clock tree to distribute clock signals to processor cores considering both clock skew and wire length minimization. Besides, on-chip interconnect wires were implemented with consideration of the latency and signal integrity. Fig. 4 shows the layout of an electronic control unit, with an area of about $10677.8um^2$. Each electronic control unit works at 1GHz clock frequency with $10.0955mw$ dynamic power under 50% switching rate.

A matched 8x8 mesh 2D electronic NoC with 5x5 input-buffered electronic routers was synthesized for comparison. The electronic router is also designed to work at 1GHz clock frequency. 32Gbit/s bandwidth for each port is offered by using 32-bit wide bidirectional metallic interconnects. Synthesis results show that the layout area of the electronic router is about $22543.7um^2$, with $11.2534mW$ dynamic power under 50% switching rate.

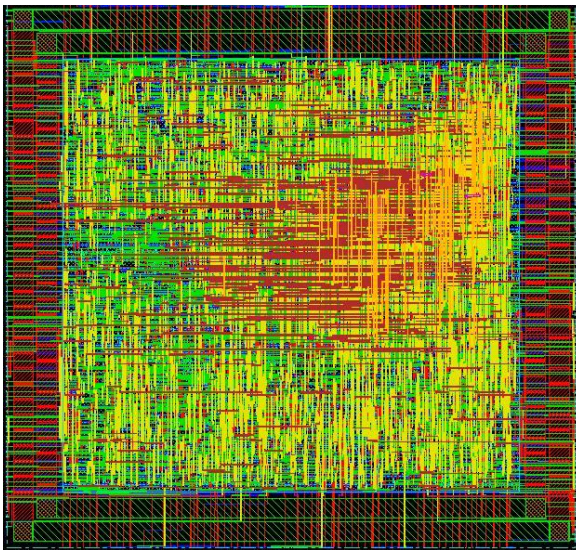

Fig. 4. Layout of electronic control unit with power ring

IV. Simulation and Comparison

Besides synthesis, the 8x8 mesh-based 3D optical NoC with 32Gbps optical link bandwidth was simulated by NS2 (a network simulator). A 12.5Gbps optical modulator based on silicon microresonator has been demonstrated experimentally in [20]. A 32Gbps optical interconnect bandwidth can be obtained by using multiple 12.5Gbps EO/OE interfaces in each injection/ejection port. The 8x8 mesh 2D electronic NoC with 32Gbps interconnect bandwidth was also simulated by NS2. Power consumption and network performance of the two NoCs were evaluated for comparison.

A. Power Analysis and Comparison

With further technology scaling, on-chip communication power is demanding an increasing proportion of the system power budget. NoC power dissipation has been such an urgent problem that optical NoC was proposed in order to reduce power consumption while delivering superior throughput. Here we compare the power consumption of the optical NoC with the matched electronic NoC based on power analytical model and synthesis results.

The total energy required to transmit a payload packet in the optical NoC is the sum of the energy cost for EO/OE conversions, the energy consumed to power on microresonators in the optical path, and the energy consumed in the electronic control network. Interfacing with 45nm CMOS circuits, energy consumed in EO/OE interfaces is about $1pJ/bit$, estimated from an 80nm technology [21]. It accounts for a large proportion of the total energy consumption. Power consumption of a microresonator in the on state is less than $20\mu W$ [12]. And it has been demonstrated in [14] that network built from Cygnus only has to power on at most three microresonators in dimensional-order routing. Such features guarantee that the maximum microresonator power consumption in our optical NoC is a small constant. In addition, the energy consumed in the electronic control network includes the energy cost to make decisions for the control packets routing and the energy consumed to transfer the control packets through metallic interconnects. Control packets are small, thus the power consumed in the electronic control network only takes a small proportion of the total power consumption.

The matched electronic NoC consumes power in several ways, including the energy required to transfer packets through the crossbars of the electronic routers, the energy consumed by the buffers, the energy required to transfer data through metallic interconnects, and the energy cost to make decisions for packets routing.

A further analysis based on synthesis results shows that for 2048B packets, the average power consumption in our optical NoC is only about $16.485nJ/packet$, while the electronic NoC consumes about $55.278nJ/packet$. The optical NoC has thus a 70% power saving for 2048B packets.

B. Network Performance Analysis and Comparison

After power analysis, network performance of the two NoCs were evaluated and compared in metrics of end-to-end (ETE) delay (Fig. 5) and network throughput (Fig. 6). ETE delay is the average time a packet takes to reach the destination. In our optical NoC, it is the sum of the path setup time and the payload transmission time. Path setup time takes a large proportion of the ETE delay. Network throughput is another important performance metric. It is the total throughput of the network under a given injection rate.

The optical NoC uses circuit switching, in which an optical path is reserved prior to the transmission of payload packets. The referenced electronic NoC uses wormhole switching, a kind of packet switching in which packets are pipelined through the network. During the simulation, functional cores were assumed to generate packets independently and the packet generating intervals followed a negative exponential distribution. We used the uniform traffic pattern, in which each source sends packets to all other nodes with the same probability. The initial 10000 clock cycles of each simulation

were run as the warm-up period to allow transient effects to stabilize. The range of packet sizes were chosen from 512B to 4096B.

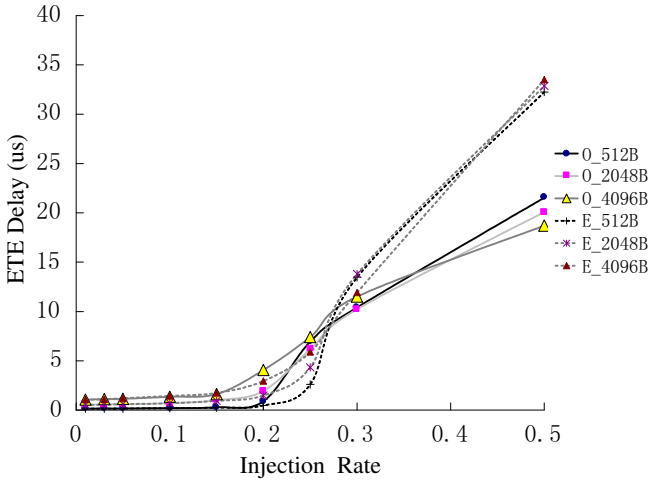

Fig. 5. ETE delay of the optical NoC and the electronic NoC

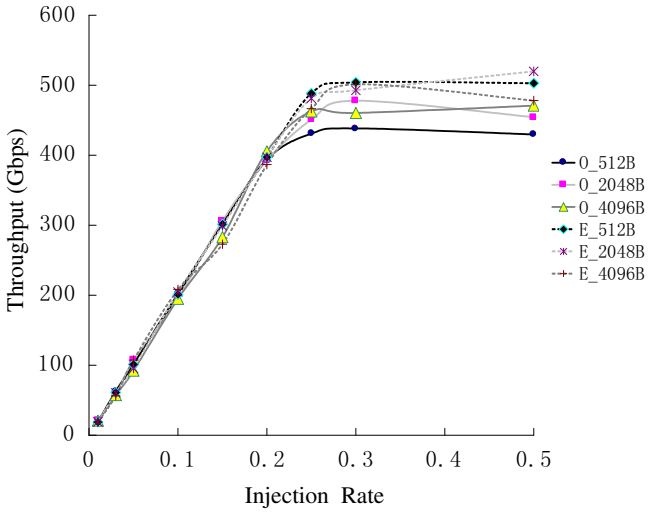

Fig. 6. Throughput of the optical NoC and the electronic NoC

The overall trend of the two NoCs performance are similar to each other. Fig. 5 shows that ETE delay increases along with the increase of injection rate. It is low at small injection rates but goes up quickly after saturation. Take 512B packets in optical NoC for example, ETE delay is less than $1\mu s$ before the injection rate 0.2, but increases dramatically after that. Network congestion is the main reason for the dramatic increasing ETE delay after saturation load. Fig. 5 also shows that after injection rate 0.3, ETE delay of the optical NoC becomes much smaller than the electronic one with the same packet size. For 4096B packets, it is $18.7\mu s$ in the optical NoC while $33.5\mu s$ in the electronic one. The optical NoC performs much better than the electronic NoC when the network becomes congested.

On the other hand, Fig. 6 shows that the throughput increases along with the increase of injection rate before saturation. After the network becomes saturated, the throughput stops increasing. For the optical NoC using 2048B packets, the throughput keeps increasing before the saturated injection rate 0.3. Its maximum throughput is about $478Gbps$. Fig. 5 and Fig. 6 also show that performance of the optical NoC is affected by the packet size. Larger payload packets correspond to less control overhead and thus lead to better performance. The optical NoC using larger packets has higher maximum throughput, but further increases in the packet size after 2048B do not increase the maximum throughout any more.

Resource utilization of circuit switching is low because all reserved resource can not be used by other packets transmission until the reserved path is teared down. Performance of the optical NoC is thus limited by the low resource utilization. Fig. 6 shows that the optical NoC maximum throughput is slightly lower than the electronic one. It also shows that as the packet size increases, the difference between them becomes smaller.

V. Conclusion

This paper proposed a 3D electronic-controlled optical NoC for MPSoC, using Cygnus optical routers. It is implemented in a TSV-based 3D chip with two device layers, taking advantage of 3D integrated circuits technology to support for the realization of the mixed technology chips. The upper device layer integrates an optical data transmission network, which connects the optical switching fabrics of all the Cygnus routers. The bottom device layer contains all of the electronic components, including electronic control units and functional cores. The electronic control units use an electronic network to route control packets and then configure the corresponding optical switching fabrics. The two device layers are stacked together with TSVs. An 8x8 mesh-based 3D optical NoC was simulated and compared with a matched 8x8 mesh 2D electronic NoC in power consumption and performance. The electronic control network of the 3D optical NoC and the traditional electronic NoC were both synthesized in a 45nm high-performance CMOS process. Power analysis based on synthesis results shows that the optical NoC can have a 70% power saving for 2048B packets. Besides, network simulation of the optical NoC evaluated the ETE delay and network throughput under varying injection rates and different packet sizes. The results show that a maximum throughput of $478Gbps$ can be offered by the 8x8 mesh-based 3D optical NoC with 32Gbps optical link bandwidth. Because of the low resource utilization of circuit switching, the maximum throughput of the optical NoC is slightly lower than the matched electronic one.

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