Negative-U Defect Passivation in Oxide-Semiconductor by Channel Defect Self-Compensation Effect to Achieve Low Bias Stress V_{TH} Instability of Low-Thermal Budget IGZO TFT and FeFETs

Chun-Kuei Chen†, Zefeng Xu†, Sonu Hooda, Jieming Pan, Evgeny Zamburg, and Aaron Voon-Yew Thean*
Department of Electrical and Computer Engineering, National University of Singapore (NUS), Singapore 117583
Singapore Next-Generation Hybrid μ-Electronics Center (SHINE), Singapore 117583.
†Equal contribution; Email: Aaron.Thean@nus.edu.sg

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***Abstract*—**In this work, we elucidate the fundamental bias stress reliability mechanism in oxide-semiconductor devices and provided guidelines to improve interface/bulk-induced V_{TH} degradation. We provide further insights into the defect-self compensation effect for the bilayer ITO-IGZO channel. Specifically, how our process approach led to effective passivation of channel defects such as negative-U defects, and ionized-oxygen-vacancy defects. With bilayer ITO-IGZO, we demonstrated 10x negative/positive bias stress (NBS/PBS), and 4x negative bias illumination stress (NBIS) improvement against the conventional mono-IGZO devices. Furthermore, under a low-thermal budget constraint, we implemented a sacrificial replacement gate stress memorization technique to enhance the ferroelectric phase to enable a double-gated (DG) IGZO FeFET. Our reliability-optimized DG ITO-IGZO FeFETs exhibit an enhanced memory window (MW) of 1.7V, excellent memory-write endurance of 10^7 cycles, outstanding memory retention with high I_{ON}/I_{OFF} of 10^6 after 10^4s, record-low NBS/PNS V_{TH} shift of 30mV, and NBIS V_{TH} shift of 110mV after stress time of 1000s. These devices set a new oxide thin-film transistor (TFT) reliability record making major strides toward highly reliable BEOL logic and memory switches.

I. Introduction

The interests in low-thermal budget beyond-Silicon back-end-of-line (BEOL) switching device solutions to augment the Si CMOS ICs platform have grown [1] the potential to realize dense monolithically 3D (M3D)-integrated logic and memory that enables dynamic system reconfigurability that can enable new hardwares for data-abundant IoT edge AI devices and non-volatile FPGAs [2]. Especially, ferroelectric FETs (FeFETs) integrated with oxide-semiconductor channels have gained significant attention for back-end-of-line (BEOL) memory-logic technology applications and M3D-ICs systems (E.g., reconfigurable CIM accelerator [3], logic-in-memory computing [4], non-volatile TCAM [5], etc.), motivated by its low-thermal-budget process and compatibility with low-resistivity Copper-low-k BEOL.

However, the gate reliability of oxide-based channel devices for logic technologies (I.e., V_{TH} stability) still needs improvement relative to the more mature Silicon CMOS technologies. This arises from the following fundamental material challenges: (1) The variety of complex channel defect types (E.g., interstitial oxygen atoms, weakly bonded oxygen, oxygen vacancies, etc.) (E.g., Excess channel and channel/high-K interface defect density ($>10^{13}cm^{-3}eV^{-1}$)). (2) The yet-to-be-clarified bias stress stability influence due to bulk channel defects versus channel/high-K interfacial defects (E.g., negative-U behavior, oxygen vacancy ionization, defect generation, etc.). (3) The defect passivation solution is still very limited, especially in the face of different process ambients (E.g., passivation of oxygen-related defects also leads to changes in channel carrier concentration) **(Fig. 1(b))**.

In this work, we address these challenges by further augmenting our previously-reported ITO-IGZO channel solution [6]. The bilayer channel approach has already been shown to trigger channel/interface defect self-compensation to passivate the deep-level bulk/interface defect density down to $10^{11}cm^{-2}eV^{-1}$. In this work, we show that our ITO-IGZO approach can further reduce the bias stress instability by 10x with respect to a mono-IGZO channel device. We provide a systematical study of the reliability degradation mechanisms in mono-IGZO channel devices and discuss the role of ITO film in suppressing channel defects such as negative-U defects and Vo ionization. This significantly minimizes the NBS/PBS-induced V_{TH} instability down to the sub-30mV range, which is highly crucial for the non-volatile logic application. We show that a highly-stable ITO-IGZO bottom-gated (BG) TFT can be integrated with a top-side ferroelectric-gate stack to enable a DG FeFET with a low maximum process temperature of only 380°C. We also implemented a ferroelectric-film-thickness stress-engineered process that further enhanced the ferroelectric phase leading to a 2x increase in ferroelectric polarization and memory window. Our DG devices show an outstanding performance against the most reported BEOL devices to date while setting a best-in-class reliability **(Table. I)**.

II. Sturcture Design of DG FeFETs

The key process steps for DG device fabrication with the device schematic diagram are depicted in **Fig. 2**. The top gate stack comprises ferroelectric HfZrOx for memory encoding, while the high-k HfOx bottom gate stack serves logic switching or memory read-out operations. Utilizing such a DG operation overcomes memory-read-write disturbance, and memory read-after-write delay by electron trapping/de-trapping, which are expected to challenge single-gated devices [2]. We report here the procedure to engineer the HZO-thickness-dependent stress to enable a replaced ITO electrode as the TG for the oxide channel. The transparent ITO gate allows us to expose the channel to top-side optical illumination, investigating the oxide-channel gate bias illumination instability. A mono-IGZO channel device is also fabricated as a control device to study the role of the ITO channel in reliability enhancement.

III. Channel Defects in IGZO TFTs

We first provide an insight into channel defect mechanisms, and investigate the bias stress reliability of the mono-IGZO devices. It has been reported from experiments [7] and density-functional theory (DFT) calculations [8] that the oxide channel exhibits two types of negative-U defects: (1) Oxygen peroxide state (PS) O_2^{2-}, and (2) Oxygen disorder state (DS) O^{2-} **(Fig. 3(a))**. The DS is found to be an intrinsically existing defect in the oxide-semiconductor channel while the PS defects are not preferentially formed in the as-deposited oxide film because of higher formation energy. The DS and PS defects, however, exhibit transition behavior under high electrical field stress. Such negatice-U defect transition will release or capture electrons, leading to the V_{TH}

instability issues for oxide-semiconductor. Two general examples are: (1). The DS will transform to PS during NBS, release electrons, and lead to a negative V_{TH} shift (2). The PS will transform to DS during PBS, capture electrons, and lead to a positive V_{TH} shift. Such V_{TH} shift is typically unrecoverable due to higher transition energy. In addition to channel negative-U defects, the channel oxygen vacancy (V_o) also exhibits ionization behavior. For example, the oxygen vacancy will be ionized during the negative bias illumination stress (NBIS), and becomes V_o^+ or V_o^{2+}. The released electron will cause the increased channel carrier concentration, and lead to an unrecoverable negative V_{TH} shift **(Fig. 3(b) and (c))**.

To investigate these two mechanisms and the well-known interface electron trapping/de-trapping in the oxide-semiconductor, we conducted the PBS and NBS tests on a mono-IGZO channel device with a stress voltage of $V_{TH} \pm 3.5V$. The result of the PBS test shows a significant positive V_{TH} shift (~360mV) in the mono-IGZO channel device. **(Fig. 4(a))**. As per-discussed, the negative-U defect transition from PS to DS during PBS will cause an unrecoverable positive V_{TH} shift. On the other hand, A positive PBS-V_{TH} shift can also be explained by the electron trapping/de-trapping at the channel-dielectric interface, which is typically recoverable [9]. Here, we find the positive PBS-V_{TH} shift is recoverable, namely dominated by the excess interface defects between IGZO and the high-k dielectric layer.

The NBS degradation mechanism is even more complicated. During the NBS test, we observed an abnormal positive V_{TH} shift in the mono-IGZO device **(Fig. 4(b))**. This can hardly be explained by the hole-interface-trapping mechanism, given that more and more studies have shown that holes can hardly move in the IGZO channel due to the high-density defects above the valence band maximum, in which holes will be captured in these trap states. Therefore, holes exhibit deficient mobility (~0.1cm^2/Vs) and can hardly drift to the interface even under a high electric field [10]. The oxygen vacancy (Vo) ionization theory cannot explain the abnormal positive V_{TH} shift because the ionized Vo will release electrons and transfer to Vo^+ or Vo^{2+}, and cause a negative V_{TH} shift during the NBS test. Similarly, a negative-U defect transformation theory fails to provide a reasonable explanation since the transformation from DS to PS during NBS will release electrons, leading to a negative V_{TH} shift. Such a positive V_{TH} shift can only be explained by the negative-U defects generation. It should be noted that the behavior of negative-U defects is not just limited to being transmitted, but also possible to being generated. During the NBS test, the DS O^{2-} defects are generated, and act as an acceptor-like defect, that captures channel electrons and causes a positive V_{TH} shift. A similar negative-U defects generation has also been reported recently in IGZO-based FETs, in which a negative V_{TH} shift was observed during a PBS test due to the generation of PS defects, which act as a donor-like defect [11].

We further investigate the NBIS reliability, in which the mono-IGZO devices are illuminated under UVA light with a strong power of 10mW/cm^2 and a stress voltage of $V_{TH} - 3.5V$. The mono-IGZO device shows a significant negative V_{TH} shift of 450mV **(Fig. 4(c))**. The negative V_{TH} shift of NBIS can be explained by two main mechanisms, which are negative-U defects transformation and V_O ionization **(Fig. 5(d))**. During the NBIS, the light-excited holes inject into the channel DS defects, become DS* (hole-injected state), and transfer to PS* (hole-injected state), in turn releasing electrons into the channel. On the other hand, the UVA light will excite the electrons of V_O, and induce the ionization of V_O to become V_O^+ or V_O^{2+}, which will lead to a negative V_{TH} shift. The recovery test proves a severe negative-U defects transformation in a mono-IGZO device, which eventually shows an unrecoverable negative V_{TH} shift after the recovery time of 10^3s **(Fig. 5(a))**. These results imply a high interface defect density, and severe negative-U behavior in conventional mono-IGZO devices, that lead to an undesired bias instability issue.

We next conduct the PBS, NBS, and NBIS tests on our ITO-IGZO devices **(Fig. 6)**. We find that the channel/interface defects can be passivated by defect self-compensation effect significantly, and show a 30mV positive V_{TH} shift after PBS. Our ITO-IGZO device also exhibits negligible negative-U defects transformation and generation, showing a sub-30mV negative V_{TH} shift after the NBS test, and a mitigated V_{TH} shift of 110mV after the NBIS test.

This implies that the reliability degradation caused by negative-U defects, Vo ionization, and interface electron trapping can be suppressed by the channel/interface defect self-compensation effect significantly **(Fig. 7)**. In the ITO film, the Sn-O exhibits a prominently higher bond dissociation energy as compared to those of the others in the IGZO channel; the Sn^{2+} ions can thus effectively passivate the as-existed DS defects and oxygen vacancy defects in the channel. Notably, since the PS defects are not preferentially formed in the as-deposited oxide film, our study shows that passivating the mid-gap DS defects is an effective way to mitigate the negative-U transition from DS to PS, and leads to a significantly improved bias stress V_{TH} reliability over a mono-IGZO device.

IV. High-reliability DG ITO-IGZO FeFETs

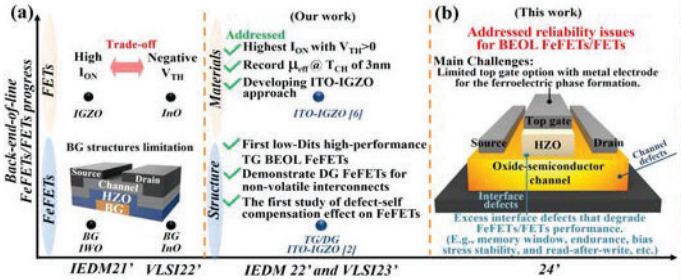
In addition to integrating the reliable ITO-IGZO channel into DG FeFETs, we also engineered the strength of in-plane tensile stress on HZO film to enhance the ferroelectric orthorhombic phase formation **(Fig. 8)**. We fabricated FeRAM with Tungsten (W) as top and bottom electrodes, and the thickness of middle-layer HZO varied from 10nm to 6nm, to investigate the HZO-thickness effects on ferroelectricity. We found a 2X increase of remnant polarization (Pr) when the HZO thickness is reduced from 10nm to 8nm. The TCAD simulation and the XRD analysis indicate that a thinner HZO thickness will lead to an enhanced tensile stress strength. It has been reported that engineering a stronger in-plane tensile stress can be an effective way to induce a stronger orthorhombic phase formation [12]. However, further scaling of the HZO thickness to 6nm will lead to a higher film leakage that degrades the Pr. Therefore, we utilize 8nm-HZO as the optimized stress-engineering thickness for our DG FeFETs.

Our DG ITO-IGZO FeFET exhibits a stable MW of 1.7V, a high I_{ON}/I_{OFF} of 10^6, an excellent endurance exceeding 10^7 cycles, and superior retention with I_{ON}/I_{OFF} of 10^6 after 10^4s. Our BG ITO-IGZO FET also shows an excellent hysteresis-free transfer curve, a high I_{ON}/I_{OFF} of 10^7, and a high I_{ON} of 10μA/μm **(Fig. 9)**.

In summary, we have provided a comprehensive study of the V_{TH}-shift degradation mechanism corresponding with different bias stress conditions, and utilize our ITO-IGZO approach to improve the reliability of the oxide-semiconductor channel. We benchmark reliability against other competitive oxide-channel devices, our PBS/NBS/NBIS-induced V_{TH} shift has reached a target corner of a minimum V_{TH} shift with the strongest stress electrical field, which sets a new record **(Fig. 10)**.

V. Conclusion

With deeper insights into the oxide-channel interface/bulk defect mechanism, we demonstrate for the first time, an effective ITO-IGZO channel approach to realize a truly reliable BEOL oxide FeFETs/FETs with the lowest PBS/NBS/NBIS-induced V_{TH} shift. Such excellent channel reliability enables the demonstrated DG FeFETs to be utilized for future non-volatile logic applications in M3D integration and edge IoT technology.



1. Excess bulk defect density as compared with conventional Si-channel.

2. Varied origins of the bulk defects include interstitial oxygen atoms, weakly bonded oxygen, oxygen vacancies, undercoordinated metals, OH-related defects, etc.

3. Complicated bulk-defects-induced reliability degradation mechanism, which is hardly distinguishable from the one induced by interface defects. (E.g., Oxygen vacancy ionization, Negative-U behavior, electron trapping/de-trapping)

4. Limited reliability optimization window due to the complexity of the bulk defects formation as a function of process ambient. (E.g., oxygen vacancy (V_o) can be shallow donors, which dominates V_{TH} and/or channel defects, leading to reliability degradation)

Fig.1. (a) The recent evolution of back-end-of-line (BEOL) FeFETs/FETs. (b) The main challenges of this work. We demonstrate the first high-reliability BEOL oxide-based FeFETs/FETs by the proposed ITO-IGZO channel approach.

	Our work		2023 VLSI [17]	2023 VLSI [16]	2022 IEDM [15]	2022 VLSI [14]	2021 IEDM [13]
	This work	2022 IEDM [2]					
Structure	TG/DG FeFETs	TG/DG FeFETs	BG FETs	BG FeFETs	BG FETs	BG FeFETs	BG FeFETs
Channel	ITO-IGZO	ITO-IGZO	In_2O_3	ZnO	IGZO	In_2O_3	IWO
Normally Off	Yes	Yes	Yes	Yes	Yes	No	Yes
MW	1.7V	0.57V	N.A.	1.5V	N.A.	2.5V	0.7V
Endurance (#)	10^7	10^7	N.A.	10^9	N.A.	10^9	10^{10}
Retention	10^6x	100x	N.A.	N.A.	N.A.	N.A.	0.3V
V_{TH} shift of PBS/NBS	30mV/30mV	N.A.	50mV/58mV	N.A.	2V/60mV	N.A.	N.A.
NBIS	110 mV	N.A.	N.A.	N.A.	N.A.	N.A.	N.A.

Benchmarking Table: Our DG ITO-IGZO device exhibits a record reliability performance against other BEOL FeFET/GETs reported to date.

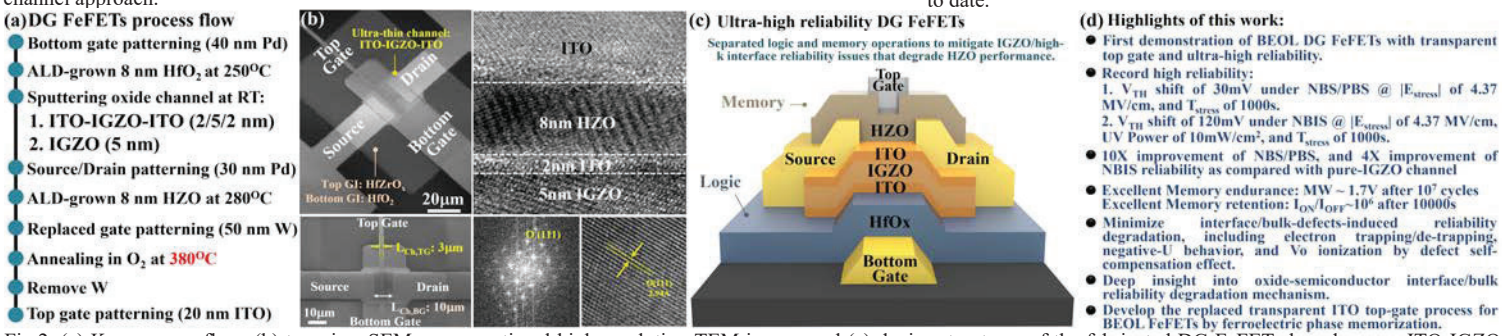


Fig.2. (a) Key process flow, (b) top-view SEM, cross-sectional high-resolution TEM image, and (c) device structures of the fabricated DG FeFETs based on our ITO-IGZO approach [6]. The TG FeFET is designed to be a memory element, while the BG FET is utilized as a logic switch. This enables our DG FeFETs to be operated as a merge memory-logic device without a memory-read-write disturbance issue. (d) Highlights of this work.

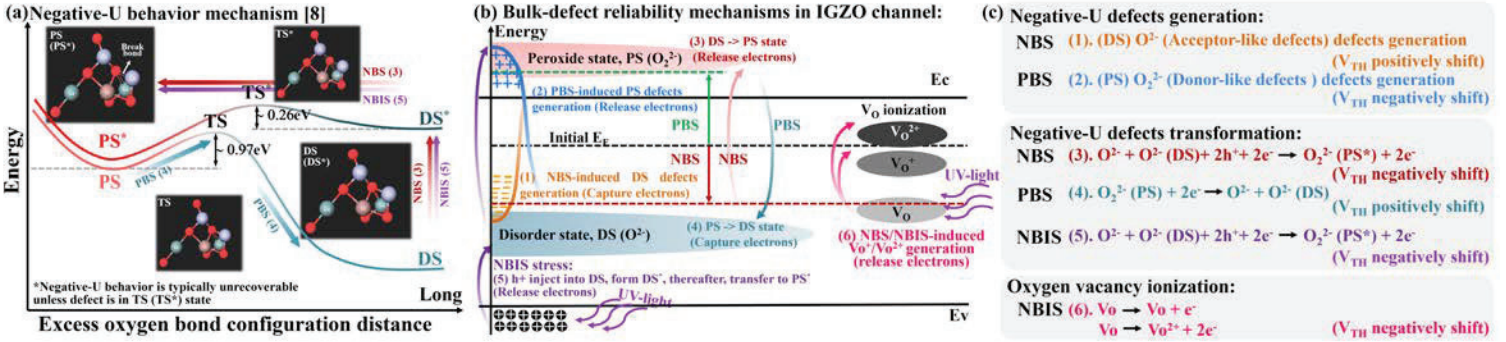


Fig.3. (a) The mechanism of the negative-U defects transformation and the respective transition energy [8]. (b) The illustrated scheme of the overall channel defect degradation mechanisms includes negative-U defects, and oxygen vacancy ionization with different bias stress test conditions (PBS, NBS, and NBIS). (c) The details of channel defect transformation or generation, corresponding with the shift of V_{TH}.

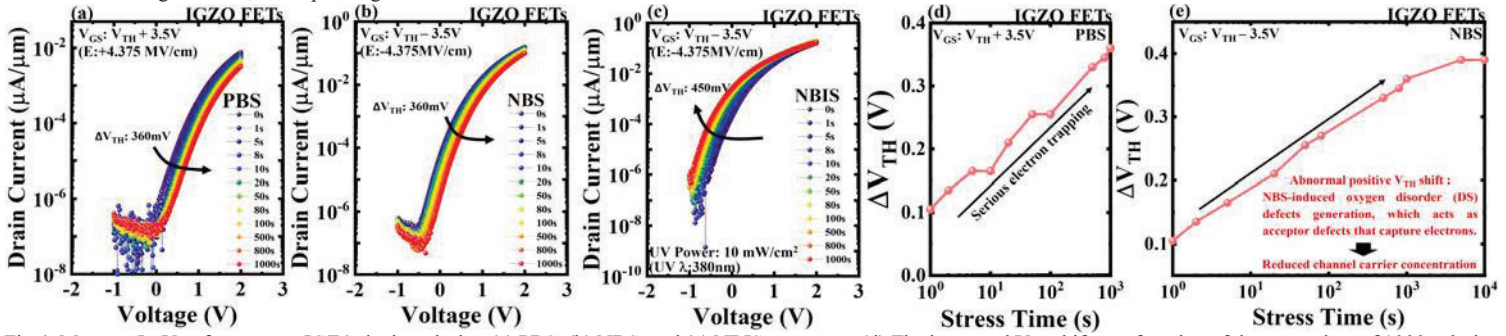


Fig.4. Measure I_D-V_G of our mono-IGZO devices during (a) PBS, (b) NBS, and (c) NBIS stress test. (d) The inspected V_{TH} shift as a function of the stress time of 1000s. during PBS, and (e) NBS test of mono-IGZO devices. The abnormal positive V_{TH} shift during the NBS stress test can be explained by negative-U defects generation.

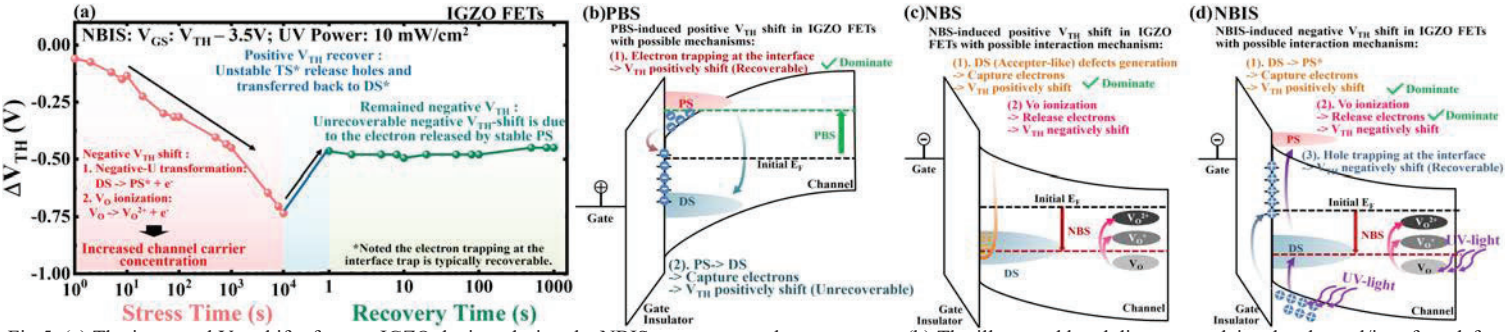


Fig.5. (a) The inspected V_{TH} shift of mono-IGZO devices during the NBIS stress test, and recovery test. (b) The illustrated band diagram explains the channel/interface defect induced-V_{TH} shift mechanisms of PBS, (c) NBS, and (d) NBIS test.

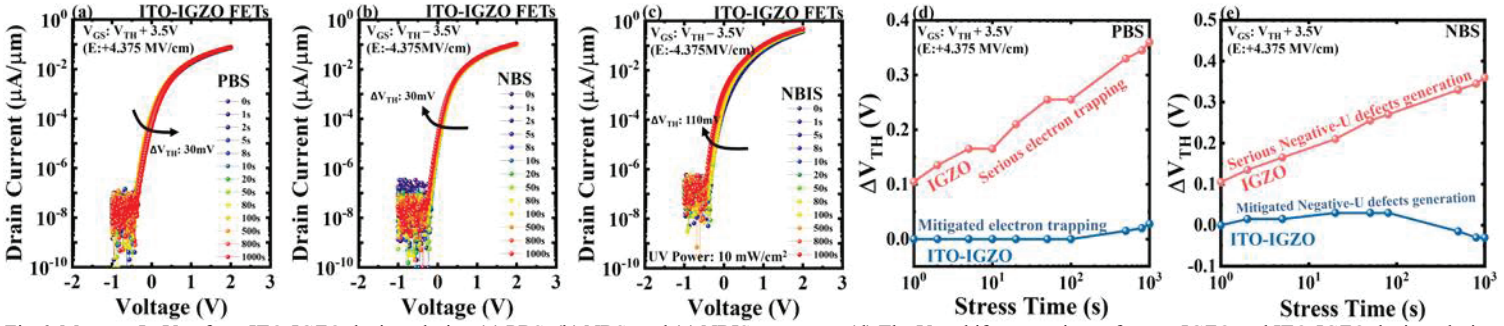


Fig.6. Measure I_D-V_G of our ITO-IGZO devices during (a) PBS, (b) NBS, and (c) NBIS stress test. (d) The V_{TH} shift comparison of mono-IGZO and ITO-IGZO devices during PBS, and (e) NBS test. We significantly mitigated electron trapping, and negative-U behavior by the proposed ITO-IGZO approach.

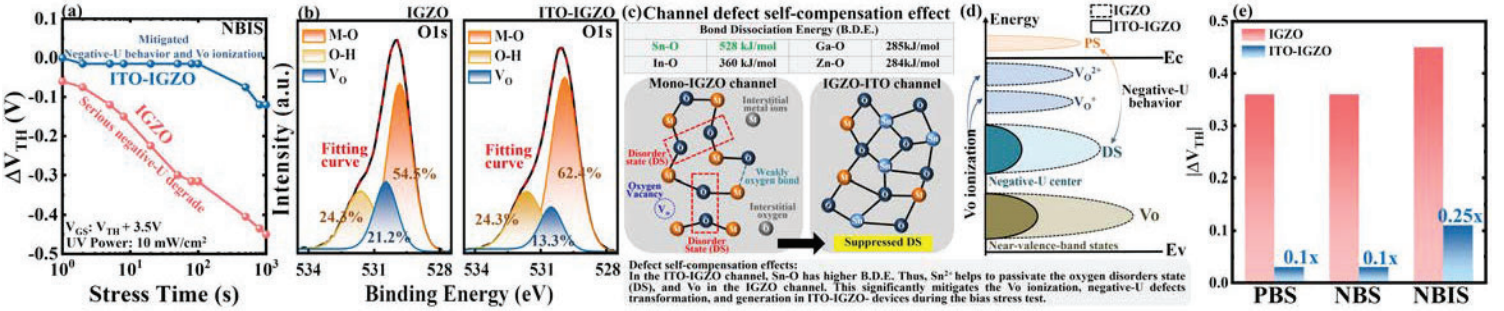


Fig.7. (a) The V_{TH} shift comparison of mono-IGZO and ITO-IGZO devices during NBIS test. (b) The O_{1s} XPS analysis indicting the enhanced M-O bonds, and mitigate oxygen vancancy in ITO-IGZO channel. (c) The mechanism of defect self-compensation effect and the illustrated density of state (DOS) of mono-IGZO and ITO-IGZO channel. The oxygen disorder state (DS) and oxygen vacancy (Vo) are highly passivated in ITO-IGZO channel. (e) The overall comparison of V_{TH} shift improvement between mono-IGZO and ITO-IGZO devices. We achieved a 10x improvement of NBS/PBS V_{TH} shift, and a 4x improvement of NBIS V_{TH} shift based on the proposed ITO-IGZO approach.

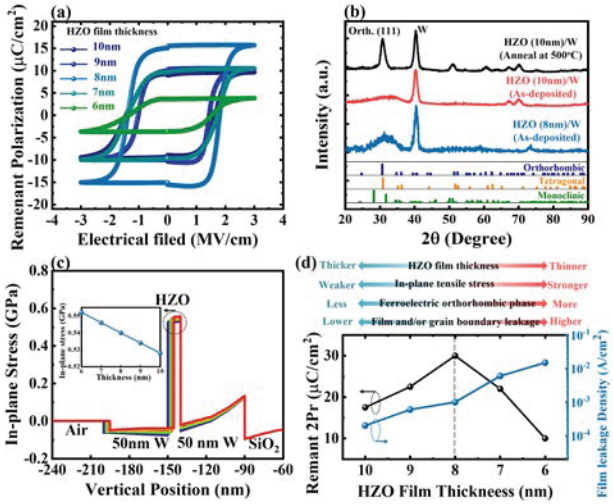


Fig.8. (a) Measured P-E curve of the fabricated Fe-RAM with different HZO thicknesses to study the tensile stress engineering. (b) GI-XRD analysis shows a stronger HZO ferroelectric crystalline orth. (111) phase peak with a thinner HZO thickness. (c) TCAD simulation results of the in-plane stress strength of different HZO thicknesses FeRAMs. (d) Measured remnant polarization as a function of HZO thickness. A stronger tensile stress can be achieved with a thinner HZO thickness while facing the trade-off of higher leakage density.

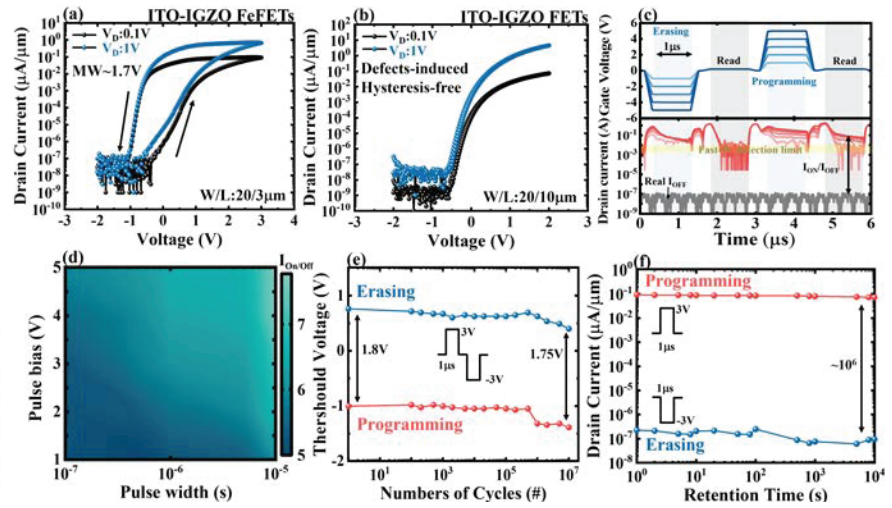


Fig.9. (a) Measured I_D-V_G of our ITO-IGZO FeFETs with transparent ITO top gate, and (b) I_D-V_G of our ITO-IGZO FETs. Our ITO-IGZO FeFETs show a large MW of 1.7V, and a high I_{ON}/I_{OFF} of 10^6. The bottom logic ITO-IGZO FETs show a defect-induced-hysteresis-free transfer curve, and a high I_{ON}/I_{OFF} of 10^7. (c) Measured memory-write operation pulse with the inspected channel current, showing an excellent control of ferroelectric memory. (d) Measured I_{ON}/I_{OFF} ratio of the DG ITO-IGZO FeFETs as a function of memory programming pulse amplitude and width. (b) Measured endurance, and retention of the DG ITO-IGZO FeFETs. Our DG devices show a high memory-write endurance exceeding 10^7 cycles, and a superior memory retention with I_{ON}/I_{OFF} of 10^6 after 10^4s.

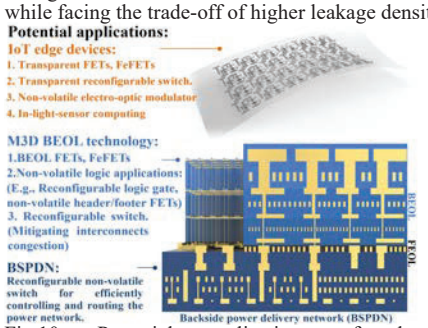


Fig.10. Potential applications of the demonstrated high reliability DG ITO-IGZO FeFET such as non-volatile electro-optic modulator at IoT edge, or reconfigurable non-volatile switch in BEOL/BSPDN.

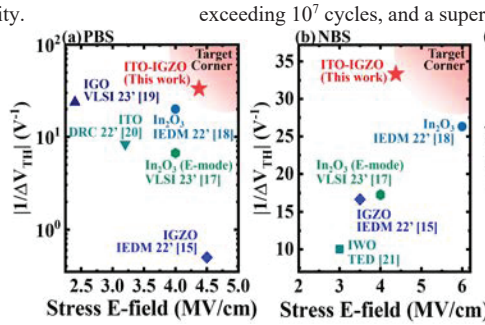


Fig.11.The benchmark of (a) PBS, (b)NBS, and (c)NBIS test reliability over other most competitive oxide-channel devices reported to date. The V_{TH} shift is benchmarked at a fixed stress time of 1000s for an effective comparison. Our ITO-IGZO devices show a significant reliability enhancement, achieving a target concer of minized V_{TH} shift with respect to the strongest stress electrical filed strength, setting a new record.

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