Haochen Yu

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About Me — I'm a Research Assistant in the Thrust of Microelectronics of the Function Hub at Hong Kong University of Science and Technology (Guangzhou), China. I have a strong passion for scientific research and am eager to learn technical skills and core competencies. Thank you for reading my CV.

Education

Master in Electronic Engineering **2022 – 2025**
Institute of Microelectronics, University of Chinese Academy of Sciences, Beijing, China

- **GPA: 3.75/4.0**
- **Related Coursework:** Computer Architecture, EDA Tools and Design-Digital Integrated Circuits, Advanced Digital Integrated Circuits, VLSI Circuits and Systems Design, Testing and Testable Design of VLSI Systems, Visual Information Processing and FPGA Implementation, Deep Learning, Intelligent Computing Systems

Bachelor in Electronic Engineering **2018 – 2022**
Nanjing University of Posts and Telecommunications, Nanjing, China

- **GPA: 3.72/4.0**
- **Related Coursework:** Principles of Computer Composition, Digital Circuits and Logical Programming, Analog Circuit Design

Projects

Robust Real-world Obeject Detection Algorithm **2022 – 2024**

- Apply evidence deep learning to single-stage multispectral object detection to achieve uncertainty expression at any image grid.
- The data distribution in the EDL object detection task was analyzed, and the EDL loss function was modified to better adapt to the real-world.
- The generalized combination with quality awareness was introduced to redistribute the probability of opinion conflicts and solve the one-vote veto problem when the mode fails.

Optimal Deployment of Detection Algorithms at Micro UAV **2024 – 2025**

- Schematic Design and PCB Layout for Video SoC
- Quantization optimization and structure optimization of algorithms for edge devices
- A complete design of wireless video transmission streams for acquisition, inference, encoding and streaming

Design of CNN Analog Computing Chip **2022 – 2025**

- Based on the principle of current integration, the design of the CNN convolution kernel calculation circuit for analog method was carried out
- Prototype design of fully connected layer digital circuits
- The layout for the analog section of the chip prototype

FPGA-accelerated Access Control Identification System **2019 – 2020**

- Design of convolutional kernel accelerated array
- FPGA-based implementation of video frame Ping-Pong buffering

Publications & Awards

- **Haochen Yu**, Rui Luo, Xiaoqin Wang, Dingyi Wang, Qiang Li, Shushan Qiao. Robust RGB-T Object Detection via Quality-aware Decision Fusion Based on Dempster-Shafer Theory. *IEEE Sensors Jounal*, 2025.
- **First Prize**, National College Students' FPGA Innovation Design Competition 2020.
- **Second Prize**, National Undergraduate Electronics Design Contest 2020.

Skills

Tools Virtuoso, DC, ICC, StarRC, PT, Calibre, Allegro, Altium Designer, Vivado

Programming Verilog, Python, Shell, C

Languages Chinese, English(TOFEL 85)